VLSI Testing

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Contents

- Introduction
- Fault Modeling
- Fault Simulation
- Test Generation
- Design for Testability
- Boundary Scan
- Built-in-Self-Test
- Memory Testing
- IDDQ testing
- CPU Testing
- System-on-a-Chip Testing
- Automatic Test Equipment
- Analog Testing
References


2. Logic Testing and Design for Testability, 1985, By Hideo Fujiwara.

3. Proceedings in ≥ 30 Conferences/Symposiums/Workshops supported by IEEE each year.

Class Requirements & Grading

- Homeworks 15%
- 6 Exercises 30%
- One Midterm Exam 25%
- One Final Exam 30%

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http://140.116.156.89/~KJLee/moe/testing_course/