Poisson Estimation

- Emphasize on transistor level and gate level.

- will cover RT-level later.

- Concentrate on static CMOS technology.

- In logic level power analysis, ASIC design style is assumed with precharacterized library data.

**Def.** A **glitch** is an incomplete signal transition on signal $S$, i.e., the voltage $V_S$ leaves from its static value and returns to its initial value without performing a full $V_{DD} - V_{SS}$ voltage swing.

![Glitch Diagram]

**Def.** A **hazard** is a useless full-swing signal transition of a signal $S$ within one clock cycle $S_i$, the signal leaves its static value, reaches the complementary value and returns to its previous static value (static hazard).
Estimation vs. Analysis.

Power estimation: a forecast of the expected power consumption of a device.

(Applied before detailed design data are available)

(Top-down design fashion)

* Used to evaluate different design alternatives.

Power analysis: calculates the power consumption of a given physical implementation.

(Bottom up process)

* Used to verify the design.
- Average power estimation (analysis)
  * Deal with average activity of the circuit
  * For calculation of average heat dissipation of the die.
  * Average battery life time.

- Worst power estimation (analysis)
  * For reliability analysis.

  Large supply current → Temporary malfunction

  IR drop
  Power rail resistance & inductance
  + Large current

  Reduced voltage
  → Cause malfunction

  Large supply current → permanent damage

  • Electromigration effects
    - E.g., bridge or open faults caused by metal migration.

Applications of power estimation & analysis.
1. Optimization for Low-power

- Design spec
  - Archi
tum 1
  - Archi
tum 2
  - Archi
tum n
  - RT-leaf 1
  - RT-leaf 2
  - RT-leaf n
  - Gate Design
  - Gate Design

- Power estimation is required. Select a good design in each level.

- Estimation can't be accurate. Can only get relative values.

2. Quality:
   - Compare specified power consumption with the achieved power dissipation

3. Reliability Analysis:
   - Electromigration: power analysis might suggest a good wire dimension
   - Hot spot: Can be avoided by power optimization (worst case)
   - Package: Select a good packaging to dissipate heat (average power)
Data dependency

- Power dissipation of a circuit depends on primary input patterns.
- Power analysis requires knowledge of typical activity at inputs (can be achieved by simulation for ASIC chips).

\* Expected Value \( E(s) \) for a signal \( s(t) \):

\[
E(s) = \lim_{T \to \infty} \frac{1}{T} \int_{t=0}^{T} s(t) \, dt \quad s(t) = 0 \text{ or } 1
\]

\[
= p(s=1) = p(s).
\]

\[ E(\bar{s}) = p(\bar{s}) = p(s=0) = 1 - p(s) . \]

\* Signal transition probability

\[
P_{st} (s(t)) = p(s(t-\delta))(1-p(s(t))) + (1-p(s(t-\delta)))p(s(t))
\]

\[
= p(s(t-\delta)) + p(s(t)) - 2p(s(t-\delta)p(s(t))).
\]

\* Signal correlations

- Uncorrelated signals
- Temporally correlated signals
- Spatially correlated signals
- Spatiotemporal correlated signals
- Structural correlation
- Sequential correlation.
Uncorrelated input signals

- Very rare
- Assume all inputs are independent.
- Assume all signals are stationary.

\[ P(s(t)) = P(s(t-t)) = P(s) \]

\[ \text{signal pdfs are the same.} \]

\[ P(s_i(t)) = P(s_i) = 2P(s_i)(1-P(s_i)) \]

\[ E(s_i) = P(s_i)(1-P(s_i)) \cdot 1 + P(1-P(s_i), P(s_i)) \cdot 1 \]

\[ = 2P(s_i)(1-P(s_i)) \]

\[ \therefore P_{out}(s_i(t)) = E(s_i) \]

\[ P(o_{AND}) = \prod_{\text{all inputs}} P(i_{AND}) \]

\[ \text{input i equals 1} \]

\[ P_{out}(o_{AND}) = 2\ P(o_{AND})(1-P(o_{AND})) \]

\[ \text{input i equals 1.} \]

\[ P(o_{OR}) = 1 - \prod_{\text{all inputs}} (1-P(i_{OR})) \]

\[ P_{out}(o_{OR}) = 2\ P(o_{OR})(1-P(o_{OR})) \]
Example:

\[
\begin{align*}
&0.5 \quad 0.25 \\
&0.5 \quad 0.75 \\
\end{align*}
\]

\[
1 - \frac{1}{4} \cdot \frac{3}{4} = \frac{13}{16}
\]

\[P_{sw} = 2 \left( \frac{1}{4} \right) \left( \frac{3}{4} \right) = \frac{6}{16} = \frac{3}{8}\]

* Spatial Correlations.

* Spatial correlation between inputs.

* Only patterns 00 and 11 can be applied to i and j.

* Both patterns are equally likely.

\[
\begin{array}{c c | c}
0 \rightarrow 1 & 0 \rightarrow 1 & 0 \rightarrow 1 \\
1 \rightarrow 0 & 1 \rightarrow 0 & 1 \rightarrow 0 \times \\
0 \rightarrow 0 & 0 \rightarrow 0 & 0 \rightarrow 0 \times \\
1 \rightarrow 1 & 1 \rightarrow 1 & 1 \rightarrow 1 \\
\end{array}
\]

\[E_{q_{sw}} = \frac{1}{2}\]

\[E_{q_{sw}} = P(0 \rightarrow 1) \cdot 1 + P(1 \rightarrow 0) \cdot 1 = \frac{1}{4} \cdot 1 + \frac{1}{4} \cdot 1 = \frac{1}{2}\]
Without the spatial correlation:

\[ \text{output} \]

6 of the changes in input cause output switching.

\[ \frac{6}{16} = \frac{3}{8} \]

Temporal Correlation

Example: Every 0 applied to \( i \) is immediately followed by 1. Every 01 applied to \( j \) is immediately followed by 0.

\[ \text{Eg}(sW) = \frac{4}{9} \]

\[ \text{Eg}(sW) = p(0 \rightarrow 2) \cdot 1 + p(1 \rightarrow 0) \cdot 1 = p(0) \cdot p(1) + p(1) p(0) = \frac{3}{8} \]
\[
\begin{array}{c|c|c}
\text{i} & \text{j} & \text{output} \\
0 \rightarrow 1 & 0 \rightarrow 0 & 0 \rightarrow 0 \\
0 \rightarrow 1 & 0 \rightarrow 1 & 0 \rightarrow 1 * \\
0 \rightarrow 1 & 1 \rightarrow 0 & 0 \rightarrow 0 \\
1 \rightarrow 0 & 0 \rightarrow 0 & 0 \rightarrow 0 \\
1 \rightarrow 0 & 0 \rightarrow 1 & 0 \rightarrow 1 * \\
1 \rightarrow 0 & 1 \rightarrow 0 & 1 \rightarrow 0 * \\
1 \rightarrow 1 & 0 \rightarrow 0 & 0 \rightarrow 0 \\
1 \rightarrow 1 & 0 \rightarrow 1 & 0 \rightarrow 1 * \\
1 \rightarrow 1 & 1 \rightarrow 0 & 1 \rightarrow 0 * \\
\end{array}
\]

* Spatiotemporal Correlation

\[
\begin{array}{c}
i \\
\downarrow \\
j
\end{array}
\]

Ex. \(i\) changes exactly if \(j\) changes.

Only patterns \(00\) and \(11\) can be applied to \(i\) & \(j\),
and \(0\) in \(i\) is immediately followed by \(1\).

\[
\begin{array}{c|c|c}
\text{i} & \text{j} & \text{output} \\
0 \rightarrow 1 & 0 \rightarrow 1 & 0 \rightarrow 1 * \\
1 \rightarrow 0 & 1 \rightarrow 0 & 1 \rightarrow 0 * \\
1 \rightarrow 1 & 1 \rightarrow 1 & 1 \rightarrow 1 \\
\end{array}
\]
Example:

```

i  j  k
0  0  0
0  0  1
0  1  0
1  1  1
```

The value of this vector depends on previous history (temporal) of each bit (spatial).

```

0 0  spatiotemporal.
```

- Structural Correlation

```

a
b

f = 0 \rightarrow c \land d = 1 \rightarrow a = 0 \downarrow e = 1
```

```

a  b  c  d  e  f
0  0  1  1  1  0
0  1  0  1  1  1
1  0  1  0  1  1
1  1  0  1  0  1
```

if $f = 0 \rightarrow e = 1$

if $e = 0 \rightarrow f = 1$
b has relation with a (spatio)

b has delay of a (temporal)

**Sequential Correlations**

\[ S_1 \rightarrow S_2 \rightarrow S_3 \]

\[ \uparrow \text{ temporal correlation.} \]
Relative Importance.

Average relative error

$$E_{\text{average}} = \frac{\sum E(sw)_{\text{accurate}} - \sum E(sw)_{\text{ignore-correlation}}}{\sum E(sw)_{\text{accurate}}}$$

Note: An overestimate of a signal can be compensated by an underestimate of another signal.

Relative signal error

$$E_{\text{signals}} = \frac{1}{\# \text{signals}} \sum_{\text{signal } i} \frac{E(sw)_{\text{accurate}} - E(sw)_{\text{ignore-correlation}}}{E(sw)_{\text{accurate}}}$$

Example: Build up a act & do simulation

- data-pack
- Controller
- Mixed CKT (data pack + controller)
Controller:

* Ignore the sequential correlation at signals state

\[
\text{Cavege} = 25\% \quad \text{Csignal} = 120\%
\]

* Ignore spatial and temporal correlations at PIs are less critical.

Data-path: No sequential elements.

* Ignore spatial and temporal correlations at PIs

\[
\text{Cavege} = 8\% \quad \text{Csignal} = 30\%
\]

Mixed (IIR Filter):

* Ignore spatial & temporal correlation at PIs

\[
\text{Cavege} = 26\% \quad \text{Csignal} = 5-6\%
\]
Conclusions:

1. Errors made for single outputs >> Errors made for average
2. Error by ignoring single correlation may hide the improvement or deterioration of optimizing transformations

Eg.

\[
\text{power} \quad \text{accurate} \quad \text{ignore the correlation}.
\]

\[
\text{design} \quad \text{harmful} \quad \text{This causes the test of power optimization.}
\]

Delay models

- Also affect the switching activity and make power analysis difficult

\[
\text{Zero delay model}
\]

\[
\text{Unwanted switching and consume power}
\]
- Delay models highly affect the hazard and glitch analysis.

- The ratio of hazardous components to the total power dissipation is about 9%~30%. (mean value of this value is 15~20%).

- Zero delay.
  - Cycle-based simulation: the value of each net is computed only once at the end of the clock cycle.
  - Hazards will not be detected.
  - For early estimation (power of Boolean functions).
  - Ignores glitch or hazard power consumption.
  - Underestimates the power dissipation.

- Finite unit delay
  - Assume a common constant delay for all gates.
  - Can generate and propagate hazards.

- Limited real application
• Real delay

• Based on cell library characterization.

• Based on pin-to-pin delay for output load and input slope.

• Should be able to handle glitch and hazard

\[ \text{Input slope} \]

\[ \text{Output load} \]

\[ \text{Gate dimensions} \]

Create table for transition time and power consumption for each cell.

• Interconnect delay dominates in deep submicron, and must be considered.

\[ \text{Interconnect delay} \]

\[ \text{Gate delay} \]

\[ 1.5 \ 1.2 \ \text{Afm} \ 45 \ 35 \]

• Should use backannotation data after layout has been available.
* power analysis (estimation)

* pattern dependent simulation techniques:
  Most commercial tools use this method.

* pattern Independent Analysis:
  Symbolic simulation
  Probabilistic simulation
  Impossible solution so far.

* pattern Independent Analysis
  will just show the concepts.

  * Symbolic simulation: calculates the switching activity of
each node from statistical properties
  * show by example: of the PIs in an analytical way.

```
\begin{align*}
p(e) &= 1 - p(a) \cdot p(b)
p(g) &= p(\bar{a}) \cdot p(\bar{b}) + p(a) \cdot p(b)
\end{align*}
```
* Impossible solution if ckt is large.
  (For medium to large ckses, the symbolic
  probabilistic simulation formulae become too large to build).

\[
\begin{align*}
\text{as} & = \frac{1}{2} \\
\text{as} & = \frac{3}{12}
\end{align*}
\]

* Use exact probability simulation for reconvergent fanout
  ckt area.

* Example:

\[
\text{Diagram of a complex circuit}
\]

* Use exact prob analysis.

* Impossible if ckt size is large.

Pattern-dependent simulation Techniques

- Most commerical tools use this approach.

- Can be done by different levels of abstraction.
- Electrical level: No library characterization required
- Abstract level: Library characterization, activity analysis, power calculation.

- Basic idea

![Diagram]

- Use spice
  - input signal slope
  - output cap, load, operating voltage

- Characterization
  - power view
  - power vectors

- RC data
  - for output load

- Transition data
  - match event vectors & power vectors

- Power calculation
  - as \[ \Sigma \text{each power vector \# of occurrence} \]
  - for all dynamic states
  - power in each state

- Power dissipation
• Exhaustive simulation
  • Brute force method
  • The total number of simulation vectors is $m \cdot 2^2$
  • Impossible solution
  • Application pattern

Try all different input transitions for each state!!!
- Statistical Simulation

- Random stimuli $\Rightarrow$ Circuit $\Rightarrow$ stop criterion

- Basic idea: for typical circuits and long observation periods, the signals behave like normally distributed stochastic variables.

- Confidence intervals
  Stopping criteria

- The total average power dissipated in a circuit during time interval $T$ is

$$P_T = \frac{V_{dd}^2}{2} \sum_{i=1}^{M} C_i \frac{n_i(T)}{T}$$

- Basic idea:
  - Random
  - Power
  - $P_T$
  - Stop if criteria satisfied
  - $T \rightarrow$ may be many clock cycles
Assume $P_T$ is normal distribution for any $T$.

- We perform $N$ different simulations, each with time $T$.
- The sample average is $\bar{P}_T$.
- Sample standard deviation $S_T$.

We have $(1-\alpha)\times100\%$ confidence that

\[
\left| \bar{P}_T - E[P_T] \right| < \frac{t_{\alpha/2}S_T}{\sqrt{N}}
\]

where $t_{\alpha/2}$ is obtained from $t$-distribution with $(N-1)$ degree of freedom.

\[
\therefore \frac{\left| \bar{P}_T - E[P_T] \right|}{\bar{P}_T} < \frac{t_{\alpha/2}S_T}{\bar{P}_T\sqrt{N}} < \frac{\epsilon}{\bar{P}_T} < \epsilon
\]

Try to control

\[
\frac{t_{\alpha/2}S_T}{\bar{P}_T\sqrt{N}} < \epsilon.
\]

\[N > \left( \frac{t_{\alpha/2}S_T}{\bar{P}_T \cdot \epsilon} \right)^2\]

- The minimum value of $N$ is

\[N \geq \left( \frac{t_{\alpha/2}S_T}{\bar{P}_T \cdot \epsilon} \right)^2\]

- Determine a minimum sample size $N$ for a specified error tolerance $\epsilon$ and a specified confidence interval $(1-\alpha)\times100\%$.
By Law of Large Numbers

\[ \text{size of sample N with mean } \mu \text{ and standard deviation } \sigma. \]

The sample will approach true mean \( \mu \) and standard deviation \( \sigma \).

\[ \sigma_T \] can be approximated by \( \sigma / \sqrt{N} \).

\[ N \] can be determined.

\[ t_{0.2} : \text{typically between 2.0 and 5.0} \]

\[ \varepsilon : \text{Constant} \]

\[ N \propto \frac{S_T^2}{\eta_T^2} \]

find \( S_T \) & \( \eta_T \) for all simulations till

\[ \frac{t_{0.2} \cdot S_T}{\eta_T \sqrt{N}} < \varepsilon. \]

Stop !!!!
• For combinational circuits, sample sizes of 20-50 might be sufficient to converge.

• Low-activity nodes may not converge fast. However, low-activity nodes do not contribute too much power consumption, any how.

• Transistor level power analysis
  - Spice
  - IRSIM
  - PowerMill

• Circuit Level — Spice (A differential equation solver).
  - Very accurate
  - Run time is prohibitive.
  - Mainly used to build up cell library.
  - How to estimate power by spice?
  - Basic idea

\[ P_{av} = \frac{1}{T} \int_{0}^{T} p(t) \, dt = \frac{V_{dd}}{T} \int_{0}^{T} i_{dd}(t) \, dt \]

\[ A \] Voltage
\[ \downarrow \]
\[ P_{av} \]

\[ \uparrow \]
\[ V_{dd} \]
\[ \downarrow \]
\[ Circuit \ under \ test \]

\[ K \cdot V_{dd} \]
\[ \downarrow \]
\[ C \]
\[ R \]
\[
C \frac{dP_{ave}}{dt} = K \cdot I_{DD}
\]

\[
P_{ave} = \frac{K}{C} \int_0^T I_{DD}(t) \, dt
\]

We just need to observe the output voltage \(P_{ave}\) above if parameters can be cleverly chosen.

\[
\frac{V_{DD}}{T} = \frac{K}{C}
\]

Note: \(R\) is only provided for DC-convergence reasons, should be chosen as high as possible to minimize leakage.

Setup:

![Diagram of the circuit with labeled components: \(U_{DD}\), \(I_{DD}\), \(P_{ave}\), \(K_{I_{DD}}\), \(C\), \(R\), \(OUT\), \(C_{load}\), \(F\).]
Example:

\[ \begin{align*}
\text{V_{in}} & \rightarrow 3 \\
3 & \rightarrow 4 \\
4 & \rightarrow \text{C_{load}} = 1 \text{pF}
\end{align*} \]

<table>
<thead>
<tr>
<th>Drain</th>
<th>Gate</th>
<th>Source</th>
<th>Subtype</th>
<th>Type</th>
<th>W</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>n_{mod}</td>
<td>10 u</td>
<td>1 u</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>p_{mod}</td>
<td>20 u</td>
<td>1 u</td>
</tr>
</tbody>
</table>

\text{U_{dd}} = 10 V

\text{Ustep} 1 4 0 ← dummy voltage source

To use a current-controlled current source, a dummy independent voltage source is often placed into the path of the controlling current.

\text{.model n_{mod} nmos}

\text{.model p_{mod} pmos}
Vin 2 0 pulse (0.5 on 2n 2n 2n 2n 2n)
Cl 3 0 1p
RP 9 0 1.0k
CP 9 0 100p

* tran in 60h uic
* print tran V(c) V(e)
* print tran i(Vtsp)
* print tran V(q)
* end

Power supply current drawn from Voo when charge-up the output capacitor.
Current Dependent Current Sources — F Elements

F element syntax statements are described in the following paragraphs. The parameter definitions follow.

Current Controlled Current Source (CCCS)

Syntax

Linear
Fxxx n+ n- <CCCS> vn1 gain <MAX=val> <MIN=val> <SCALE=val> <TC1=val>
+ <TC2=val> <M=val> <ABS=1> <IC=val>

Polynomial
Fxxx n+ n- <CCCS> POLY(NDIM) vn1 ... vnndim <MAX=val> <MIN=val>
+ <TC1=val> <TC2=val> <SCALE=vals> <M=val> <ABS=1> P0 <P1...>
+ <IC=vals>

Piecewise Linear
Fxxx n+ n- <CCCS> PWL(1) vn1 <DELTA=val> <SCALE=val> <TC1=val> <TC2=val>
+ <M=val> x1,y1 ... x100,y100 <IC=val>

Multi-Input Gates
Fxxx n+ n- <CCCS> gatetype(k) vn1, ... vnk <DELTA=val> <SCALE=val> <TC1=val>
+ <TC2=val> <M=val> <ABS=1> x1,y1 ... x100,y100 <IC=val>

Delay Element
Fxxx n+ n- <CCCS> DELAY vn1 TD=val <SCALE=val> <TC1=val> <TC2=val>
+ NPDELAY=val

Parameter Definitions

ABS
Output is absolute value if ABS=1.

CCCS
the keyword for current controlled current source. Note that CCCS is a reserved word and should not be used as a node name.
**DELAY**

Keyword for the delay element. The delay element is the same as a current controlled current source except it is associated by a propagation delay TD. This element facilitates the adjustment of propagation delay in the macromodel process. **Note:** DELAY is a reserved word and should not be used as a node name.

**DELTA**

Used to control the curvature of the piecewise linear corners. The parameter defaults to 1/4 of the smallest breakpoint distances. The maximum is limited to 1/2 of the smallest breakpoint distances.

**Fxxx**

Current controlled current source element name. The parameter must begin with an “F”, followed by up to 1023 alphanumeric characters.

**gain**

Current gain

**gatetype(k)**

Can be one of AND, NAND, OR, or NOR. (k) represents the number of inputs of the gate. The x’s and y’s represent the piecewise linear variation of output as a function of input. In the multi-input gates, only one input determines the state of the output. The above keyword names should not be used as a node name.

**IC**

Initial condition: the initial estimate of the value(s) of the controlling current(s) in amps. If IC is not specified, the default=0.0.

**M**

Number of element in parallel

**MAX**

Maximum output current value. The default is undefined and sets no maximum value.

**MIN**

Minimum output current value. The default is undefined and sets no minimum value.

**n+/-**

Positive or negative controlled source connecting nodes
NDIM polynomial dimensions. If POLY(NDIM) is not specified, a one-dimensional polynomial is assumed. NDIM must be a positive number.

NPDELAY sets the number of data points to be used in delay simulations. The default value is the larger of 10 or the smaller of TD/tstep and tstop/tstep.

That is,

\[ NPDELAY_{\text{default}} = \max\left(\frac{\min(TD, tstop)}{tstep}, 10\right) \]

The values of tstep and tstop are specified in the .TRAN statement.

P0, P1 ... when one polynomial coefficient is specified, Star-Hspice assumes it to be P1 (P0=0.0) and the source is linear. When more than one polynomial coefficient is specified, the source is nonlinear, and P0, P1, P2 ... represent them.

POLY polynomial keyword function

PWL piecewise linear keyword function

SCALE element value multiplier

TC1, TC2 first and second order temperature coefficients. The SCALE is updated by temperature:

\[ \text{SCALE}_{\text{eff}} = \text{SCALE} \cdot (1 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2) \]

TD time delay keyword

vnl ... names of voltage sources through which the controlling current flows. One name must be specified for each dimension.
x1,... controlling current through vn1 source. The x values must be in increasing order.

y1,... corresponding output current values of x

Examples

F1 13 5 VSENS MAX=+3 MIN=-3 5

This example describes a current controlled current source connected between nodes 13 and 5. The current that controls the value of the controlled source flows through the voltage source named VSENS (to use a current controlled current source, a dummy independent voltage source is often placed into the path of the controlling current). The defining equation is:

\[ I(F1) = 5 \cdot I(VSENS) \]

The current gain is 5, the maximum current flow through F1 is 3 A, and the minimum current flow is -3 A. If \( I(VSENS) = 2 \) A, \( I(F1) \) would be set to 3 amps and not 10 amps as would be suggested by the equation. A user-defined parameter can be specified for the polynomial coefficient(s), as shown below.

```
.PARAM VU = 5
F1 13 5 VSENS MAX=+3 MIN=-3 VU
```

The next example describes a current controlled current source with the value:

\[ I(F2) = 1e-3 + 1.3e-3 \cdot I(VCC) \]

F2 12 10 POLY VCC 1MA 1.3M

Current flow is from the positive node through the source to the negative node. The direction of positive controlling current flow is from the positive node through the source to the negative node of vnam (linear), or to the negative node of each voltage source (nonlinear).

Fd 1 0 DELAY vin TD=7ns SCALE=5

This example is a delayed current controlled current source.

```
Filim 0 out PWL(1) vsrc -1a,-1a 1a,1a
```

The final example is a piecewise linear current controlled current source.
Logic Level Power Estimation

* Entice-Aspen developed by Motorola.

Circuit Simulation

Entice Characterization

Entice Database

(Extracted from layout)

Interconnect RC

Circuit Netlist

Test patterns

Aspen

Logic Simulation

(2) Cell dimension & structure

0 Cell library parameters e.g.
* input signal slope
* output slope
* output capacitance load operating voltage
* power dissipation
* delay

* temperature & process variation

Circuit activity

Power activity

Floor planning
power characterization in Entice

- **Entice**: Cell characterization system that models power and timing delays.

![Diagram of a circuit with labels a, b, and c, and a pin-to-pin delay arrow pointing from a to c.]

- **Delay** through a cell depends on:
  - Supply voltage, input signal slope, output loading,
  - Operating temperature, fabrication process variation.

- **Power dissipation** also depends on the same factors.

- Support different modeling styles:
  - Polynomials, tabular data, piecewise-linear

  **Example:**
  
<table>
<thead>
<tr>
<th>a</th>
<th>0.5ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>b</td>
<td>1</td>
</tr>
<tr>
<td>c</td>
<td>0.2ns</td>
</tr>
</tbody>
</table>

  **Table:**
  
<table>
<thead>
<tr>
<th>Voltage</th>
<th>Input Waveform</th>
<th>Output Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>0V</td>
<td>1000pF</td>
</tr>
<tr>
<td>High</td>
<td>3.3V</td>
<td>500pF</td>
</tr>
</tbody>
</table>

  Can be represented by polynomial or table or...
* Power vectors: discrete all possible power events of a cell.

\[ \text{Different loading} \]

- Delay vectors — used to calculate output slope which will be used as input slope for next gate.

\[ \text{Different slope} \]

Power Analysis by Aspen

- Use Verilog XL: a logic simulator from Cadence
  * can simulate delay for each gate, based on backannotation

* 3 types of power dissipating are considered:

  Dynamic

    \[ \{ \text{Capacitive charging/discharging} \] 
      \[ \text{Short-circuit} \] 

  Static

    \[ \{ \text{Static leakage power} \] 

\[ \text{Capacitive charge} \]

\[ \text{Short-circuit} \]

\[ \text{Leakage} \]

\[ \text{Dynamic power vector} \]

\[ \text{Static power vector} \]
- Capacitive charge & discharge: use dynamic power vectors

  \[
  CV^2f
  \]

  \[
  \uparrow \quad \uparrow
  \]

  Output the frequency of charge & discharge for T.

  \[
  \text{Load}
  \]

  (Derived by logic simulation)

  \[
  \text{Input capacitance of the load}.
  \]

  \[
  \# \text{ of transitions}
  \]

  (Short Ckt)

- Transition power dissipation:

  Use dynamic power vectors.

- Derived by:
  - Check power vector
  - Check delay vector
  - Check the output slope

- Leakeage power: depends on Ckt state.

- Check the power vector.

- And set the power dissipation.
- When a net toggles, all cell instances incident to the net are examined.

- Simulation

  \[
  \text{cut} \quad \text{find a toggle} \quad \text{all logic values are gathered as an event vector.} \\
  \text{check the power vector}
  \]

- Get the power consumption from cell library

- Do not consider glitch a hazard

- Accuracy is within 10\%, when compared with Spice.

- During simulation, the number of matches between even vectors & power vectors is calculated.

- Dynamic energy consumption:

  \[
  \sum_{i} \left( \frac{\# \text{power vector } i \text{ matched}}{\# \text{power vector } i} \right) \times \text{power consumption for power vector } i
  \]

- Static energy consumption:

  \[
  \sum_{i} \left( \frac{\# \text{static power vector } i \text{ matched}}{\# \text{static power vector } i} \right) \times \text{power consumption for power vector } i
  \]

  \text{includes dynamic + short ckt power + static power consumption} \times \text{actuation time}