Low-Power VLSI Circuit Design

Final Test, Winter 2007

Each question is worth 17 points

1. Bus inversion coding can be used for interconnect data transmission with long wires. Assume the bus contains n bits and the data transmitted is uniformly distributed. Analysis shows that the power ratio with and without bus conversion can be represented by Equation (1) shown below. It can be observed that as the value of n increases, the power saved is almost 0. How to extend the idea of bus inversion to get a reasonable power saving? You must show your idea by a simple figure plus a small paragraph of explanation (DO NOT WRITE THESIS).

Equation (1)

2. Multiplying a signal with constant coefficients is a very common operation in DSP. Consider the example in which a multiplication with a constant is decomposed to IN+IN>>7+IN>>8 where **a>>b** means the value of **a** shifted right **b** bits and IN is a n-bit number. Assume the shifter is implemented by a combinational circuit, instead of a shift register, to simplify this problem. Assume you are given two adders (each adder is a n-bit adder) and two shifters (one for 7 bits while the other one for 8 bits). Show how to design this low-power multiplication by using these two adders and two shifters to implement IN+IN>>7+IN>>8. Just show block diagram design, i.e., adders and shifters are circuit blocks here. You do not need to design them. This is RT-level low-power design.

3. Given two interconnects as shown in Fig. Fig. 1(a) and Fig. 1(b). The capacitance and resistance of a fat segment of size LxW is 20 fF and 50 Ohm, respectively. The load capacitances are shown in the figures. (A) Use the Elmore delay model to calculate the delay for each interconnect. To simplify your analysis, we assume the driver gate does not contribute any parasitic capacitance and resistance. Also, try to use T-model to represent each interconnect segment. (B) Calculate the dynamic energy consumption for each transition. (C) Use this example to verify the monotone property of the interconnect sizing.

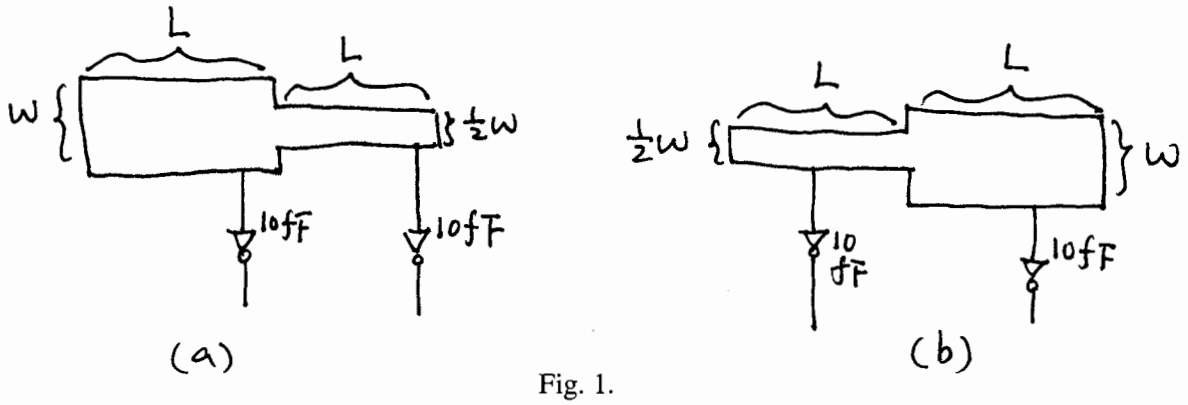

Fig. 1.

4. Assume inverter G drives n other gates as shown in Fig. 2. The best sizing W of G can be represented by Equation (2) as shown below. Equation (3) is used to derive Equation (2). (A) If the channel width of all gates driven by G is doubled, which parameter in Equation (2) will be changed? (B) If the mobility of N-type transistor is doubled, and the input of G is a falling transition, how will the optimized size W be changed? (C) If the switching frequencies of all gates are doubled, how will the optimal size W be changed?

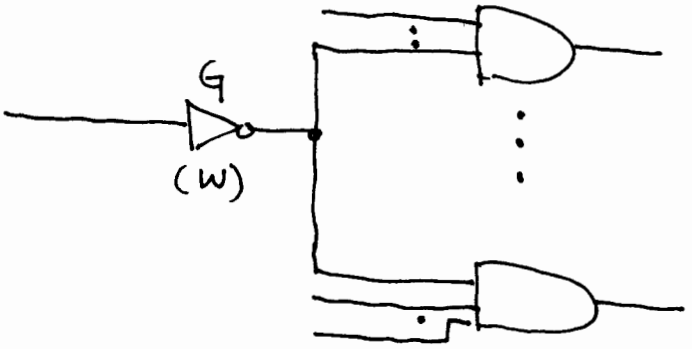

Fig. 2.

$$W = \frac{\sqrt{\phi \left(\frac{u'}{u}\right) C_L \left(\sum_{i=2}^{n} w_i f_i\right)}}{\sqrt{\left(\frac{k_1}{k} + u\tau_{in}\right) f}}$$

Equation (2).

$$P = P_1 + (kU\tau_{in} + K_1) wf + ku' \sum_{i=2}^{n} w_i f_i \left(\phi \frac{C_L}{uw} + k_2 \tau_{in}\right)$$

Equation (3).

5. Fig. 3(a) shows a memory array with size 100 rows and 100 columns. Assume the power consumed to activate each word line is P(wl), while the power consumed to activate each pair of bit lines is P(bl). Assume a low-swing bit line technique is used, so we have P(wl)=100P(bl). Now, assume the entire array has been partitioned into four banks as shown in Fig. 3(b). Also, the data has been arranged in such a way that the probability of accessing each part of every bank is prob(1) to prob(4) as shown in Fig. 3(b). Assume we have prob(1)=1/2, prob(2)=1/4, prob(3)=1/8, and prob(4)=1/8. Assume the banking will not introduce any power overhead (i.e., the extra decoder and all required extra interconnects consume little power and can be ignored). How percentage of power can be saved due to this banking. Use equation [P(without banking) – P(with banking)] / P(without banking).

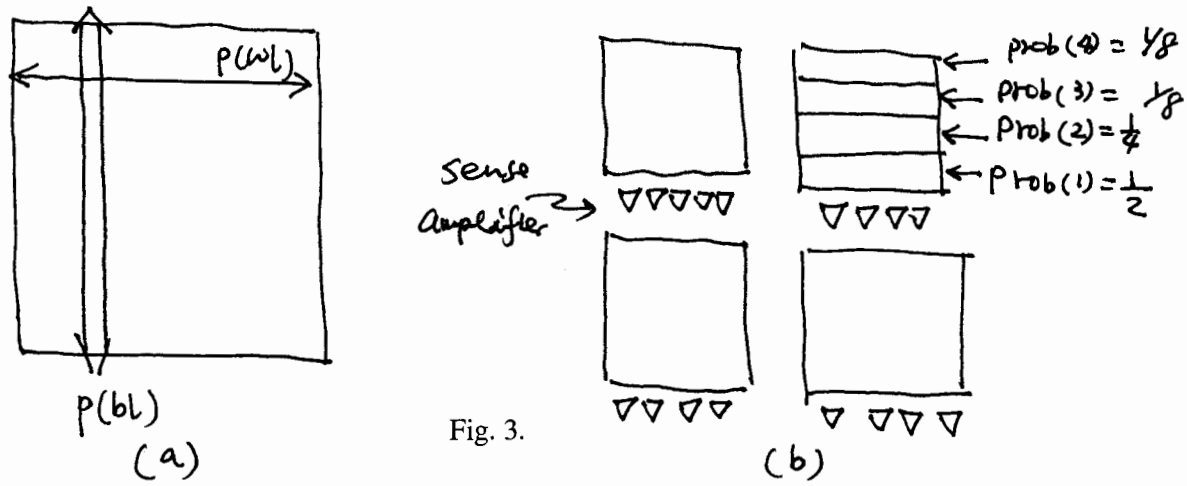

Fig. 3.

6. Fig. 4 gives the circuit of a low-leakage memory cell using data retention gated-ground cache design. (A) Based on the given memory cell state, when the cell is driven into sleep mode, which transistors will have stacking effect? (B) Add extra circuit to guarantee that stack effect can be applied to all paths from Vdd to Vgnd for each cell.

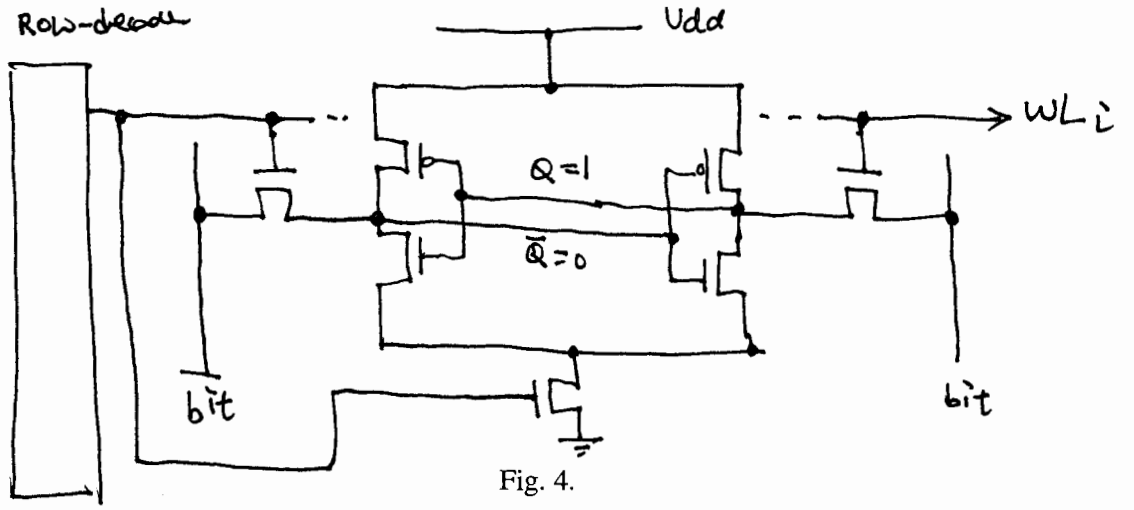

Fig. 4.

L.P. Solution Final Exam 2007 Winter

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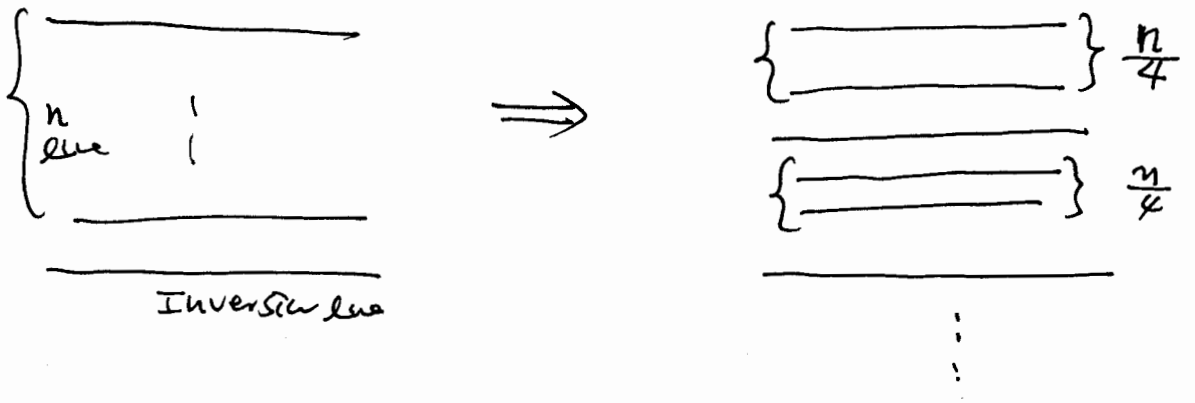

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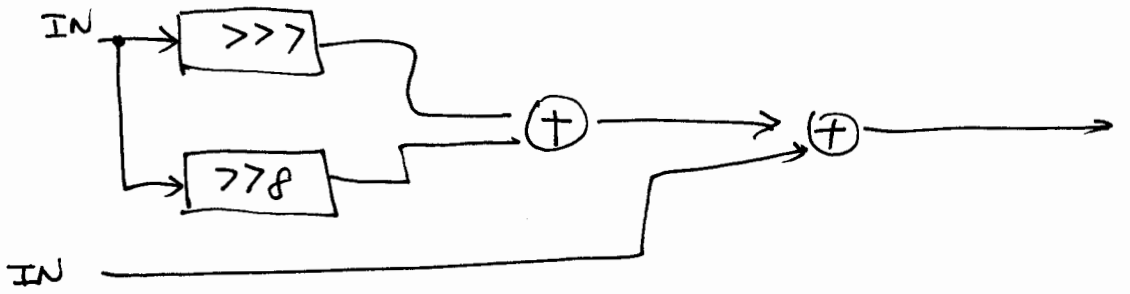
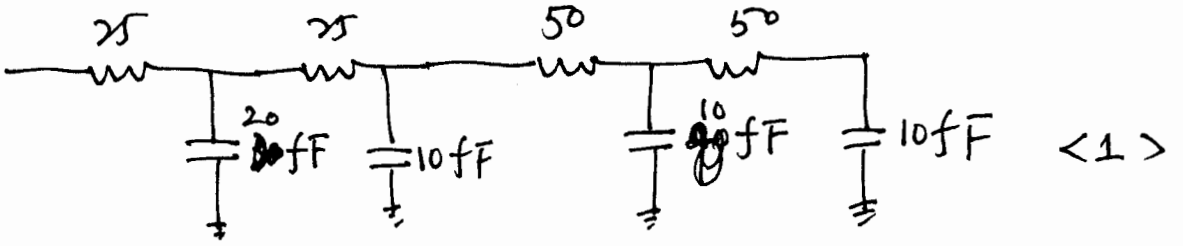


P(1)

(3)

(a)



<1>

$25(50) + 25(30) + 50(20) + 50(10)$

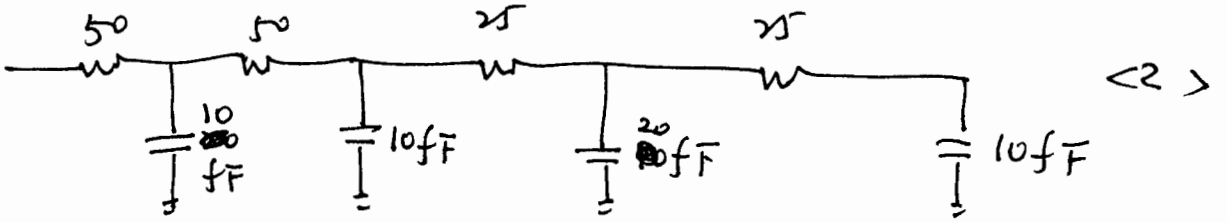
$= 1250 + 750 + 1000 + 500 = 3500$

1250
750
1000
500
3500

10^{-15}

$= 3.5 \times 10^{-12}$

3.5 pJ



<2>

$50(50) + 50(40) + 25(30) + 25(10)$

$= 2500 + 2000 + 750 + 250 = 5500$

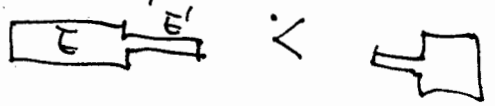
2500
2000
750
250
5500

5.5 pJ

(b)

<1>:
<2>: $C_L V_{dd}^2 = 50\, V_{dd}^2$

(c)



$<$

∴ if E' is the downstream of E,

then width (E) is no smaller than width (E').

(P2)

(4)

(A) W_i will be doped, C_L

(B) $W \longrightarrow \sqrt{2}W$

(C) the same

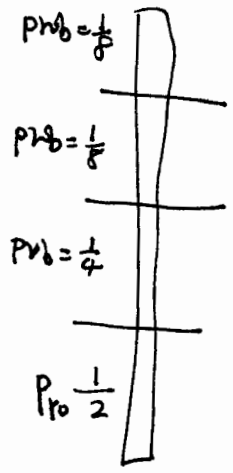
(5) Non-banked Array design $= P(WL) + 100\,P(bl) = x + x = 2x$

Banked design : $P(WL) \longrightarrow \frac{1}{2} P(WL)$

P(WL) — 4 ports

P(BL) — 2 ports

Compare 3



Let original bit power consumption be y.

partial bit line

$$\frac{1}{2} \times \frac{1}{8} y + \frac{1}{4} \cdot \frac{1}{4} y + \frac{1}{8} \cdot \frac{3}{8} y + \frac{1}{8} \frac{1}{2} y$$

$$= \frac{1}{8} y + \frac{1}{8} y + \frac{3}{32} y + \frac{1}{8} y$$

$$= \frac{4+4+3+4}{32} y = \frac{19}{32} \times \frac{1}{2} y.$$

$$= \frac{19}{64}$$

$$y = \frac{1}{100} x$$

garbage +3

(P3)

Banky total power:

$$\frac{1}{2}x + \frac{50}{100}P(b) = \frac{1}{2}x + 100 \cdot \frac{19}{64}y$$

$$= \frac{1}{2}x + \frac{50}{100}\cdot\frac{19}{64}\cdot\frac{1}{100}x$$

$$= \frac{1}{2}x + \frac{19}{64\times 2}x$$

$$= \frac{64+19}{128}x = \frac{83}{128}x$$

power saved:

$$\frac{2x - \frac{83}{128}x}{2x} = \frac{64\cdot\frac{256-83}{128}x}{64\cdot 256}$$

$$= \frac{173}{256}$$

$$\approx 67\%$$

$$\begin{array}{r} 0.45 \\ 64\overline{)29.0} \\ 256 \\ \hline 340 \\ 320 \\ \hline 200 \end{array}$$

$$\begin{array}{r} 64 \\ 25.5 \\ \hline 38.5 \end{array}$$

$$\begin{array}{r} 0.6 \\ 64\overline{)38.5} \\ 384 \\ \hline \end{array}$$

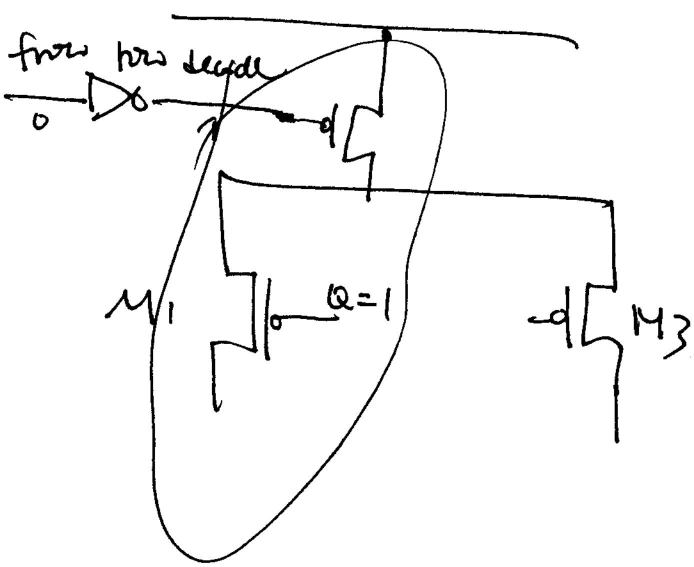
$$\begin{array}{r} 0.67 \\ 256\overline{)173.0} \\ 1536 \\ \hline 1940 \end{array}$$

PY

(6)

(A) M4 and M7, (including M6) 9

(B)



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garbage (4) 3