

Digital System Design – Spring 2008

Assignment 9: Due 6/4/08

Textbook page 673, Problem 7.64.

Design the *Fibonacci number generator and detector* as described in the textbook, except that no ABEL, VHDL, or Verilog program will be written. Design the machine with $n=8$. You can use some basic components such as counters, registers, adders or any logic gates. (a) You should first show the basic components that are required for the data path and also show the relationship between the components as what we have done for ADD-SHIFT unsigned multiplier, (b) Identify the required control signal for the components in the data path, and (3) Show the state diagram of the controller.