## on when

 $V_{\text {IN }}$ is lowon when $V_{\text {IN }}$ is high
uits that makes 3-12, different ct their logical I current flows yate; this seems behavior. It is $s$ gate indicates

IOS. A $k$-input
1put is LOW, the ecorresponding the correspond-


Figure 3-14 Switch model for CMOS 2-input NAND gate: (a) both inputs LOW: (b) one input HIGH; (c) both inputs HIGH.
ing "off" $n$-channel transistor. If both inputs are HIGH, the path to $V_{\mathrm{DD}}$ is blocked, and $Z$ has a low-impedance connection to ground. Figure 3-14 shows the switch model for the NAND gate's operation.

Figure 3-15 shows a CMOS NOR gate. If both inputs are LOW, then the output $\mathbf{Z}$ has a low-impedance connection to $V_{\mathrm{DD}}$ through the "on" $p$-channel transistors, and the path to ground is blocked by the "off" $n$-channel transistors. If either input is HIGH, the path to $V_{\mathrm{DD}}$ is blocked, and $Z$ has a low-impedance connection to ground.
(a)
(b)

| $A$ | $B$ | $Q 1$ | $Q 2$ | $Q 3$ | $Q 4$ | $Z$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $L$ | $L$ | off | on | off | on | $H$ |
| $L$ | $H$ | off | on | on | off | $L$ |
| $H$ | $L$ | on | off | off | on | $L$ |
| $H$ | $H$ | on | off | on | off | $L$ |



Figure 3-15 CMOS 2-input NOR gate:
(a) circuit diagram;
(b) function table;
(c) logic symbol.
(c)


