3.3 CMOS Logic 91



Figure 3-14 Switch model for CMOS 2-input NAND gate: (a) both inputs LOW; (b) one input HIGH; (c) both inputs HIGH.

ing "off" *n*-channel transistor. If both inputs are HIGH, the path to V_{DD} is blocked, and Z has a low-impedance connection to ground. Figure 3-14 shows the switch model for the NAND gate's operation.

Figure 3-15 shows a CMOS NOR gate. If both inputs are LOW, then the **output Z** has a low-impedance connection to V_{DD} through the "on" *p*-channel **transistors**, and the path to ground is blocked by the "off" *n*-channel transistors. If either input is HIGH, the path to V_{DD} is blocked, and Z has a low-impedance **connection** to ground.



Figure 3-15 CMOS 2-input NOR gate: (a) circuit diagram; (b) function table; (c) logic symbol.

on when $V_{\rm IN}$ is low

on when $V_{\rm IN}$ is high

uits that makes 3-12, different ct their logical l current flows gate; this seems behavior. It is s gate indicates

10S. A k-input

put is LOW, the corresponding the correspond-

Q3	Q4	Z
off	on	н
on	off	Н
off	on	н
on	off	L

Z