Automatic Test Equipment

- General introduction
  -- IC category
  -- Tester category
- ATE Hardware system
- Tester example -- DRAM
IC category

**Memory**
- Embedded:
  - DRAM
  - Flash
  - SRAM

**Analog**
- Audio/Video
  - Comm: ADCs, DACs, CODECs, PLLs, RAMDAC

**Communications**
- Fire Wire
- Fibre
- Channel
- Ethernet
- SONET
- Cable
- Modems
- ATM
- DSL
- RF

**High-speed Buses**
- RAC™
- APG-4X
- LVDS
- SCSI
- PanelLike™
- Rambus
- DDRAM

**Digital**
- Embedded:
  - MPUs
- MPEG encoders/decoders
- PC-on-a-Chip
- PCI core
- DSP
- Graphics
  - Accelerators/Controllers
Tester category

Digital
- DSP, ASIC, CBIC, ASSP, High pin-count gate Array, MPU, ASIC, SOCRISC, CISC.....

Mixed-Signal +DC Parameter
- Communications, Converters, Interface, Integrated Signal Processing, Smart Power, and Specialty.....

Memory
- DRAM, ROM, SRAM, SDRAM, Flash Memory, DDR RAM, Rambus,.................
Tester category & Examples (Advantest)

SOC Test System - MPU, ASIC, SOCRISC, CISC…… T6682 SOC Test System

VLSI Test System - ASIC, CBIC, ASSP, High pin-count gate array…… T3347B VLSI Test System

Memory Test System - DRAM, DDR, RDRAM, SLDRAM, PBSRAM…… T5591 Memory Test System

Flash Memory Test System - Flash Memory….. T5721 Flash Memory Test System

Mixed-Signal Test System - Mixed-Signal devices for audio/video, CD-ROM or other PC peripherals, mobile telephone system…… T7323 Mixed-Signal Test System

RFIC Test System - RFIC used in various types of radio communications…… T7610 RFIC Test System

LCD Drive/Panel Test System - LCD Drive IC, Looking straight type…… T7313 LCD Drive/Panel Test System

E-Beam Test System - …… E1380A E-Beam Test System
Digital Test function Diagram

Digital Master Sequencer

Vector Memory

Fall Memory

Real-Time Comparator

Receive Formatter

Drive Formatter

Edge Timing

Digital Capture Memory

MUX Time Measure

DC Test Unit

Test Vector Generator

Pin-Electronic

Drive

TR

High

Low

Active Load

PMU

DUT Pins

Synchro-Pipe
### DC Resources

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<td></td>
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<td>-7 to +8V +/-30mA</td>
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<td><strong>PVS</strong></td>
<td>Precision Voltage Source</td>
<td>23 bit Resolution</td>
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<td>0-1</td>
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<td></td>
<td></td>
<td>+/-10nV to +/-200V</td>
</tr>
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</table>
Analog Waveform Generation

- Synchro-Pipe
  - Clock
  - Dual Clock

- AWG Sequencer
- AWG
- Waveform Source Memory
- SFG
- DC Offset
- Amp/Filter
- Mux

For 30MHz / 1MHz / 100KHz AWG
- Testhead
- Testhead #1
- Testhead #2

For 128MHz AWG

Full Feature Set
- Synchronous or Asynchronous Clocking
- Triggering
- Waveform Sequencing
- Single-Ended or Differential
- Filters
- Offset
- Real-Time DSP

Digital output
Digital input
AWD Sequencer control
AWD output
Analog Waveform Digitization

- Clock
- Digitizer Sequencer
- Waveform Digitizer
- Amp/Filter
- Mux
- Waveform Capture Memory
- Synchro-Pipe
- Dual Clock
- Testhead #1
  - Filter Sampler
- Digital Point
  - Initial Discard
  - Trigger from Digital Master
  - Start
  - Total Sample Number
  - Memorizing into the Waveform Capture Memory
  - * Last Add = First Add + 1
- Waveform Capture Memory
  - First Address
  - Last Address
Time Measurement Resources

TM
Time Measurement Unit

Measurement:
- Max. 100MHz interval/period
- Max. 10ps resolution (interval)
- Max. 10fs resolution (period)
- One shot or averaging

TIA
Time Interval Analyzer

Measurement:
- Max. 80MHz interval
- Max. 50ps resolution
- Multiple sequential (max. 2\textsuperscript{nd})
- Hardware histogram functions

Single Channel
Dual Channel
Test Example -- DRAM

Architecture of DRAM

Address

Address latch → Column decoder → Memory cell array

Row decoder → Sense amplifiers

Refresh

Refresh logic → Write driver → Data register

Data flow

Data out → Data in

Control flow

Read/write & chip enable
Test Program / Test Flow

- Main program
  - Set Test Conditions
    » Timing setup
      Test Rate, Drover Clock, I/O Drive Enable clock....
    » Voltage setup
      Driver, Comparator, Terminator, Program Load, Device power, DC Measure Unit.....
    » Pin Status setup
      Pin => Voltage, Timing, Waveform, Pattern Assignment
  - Control Test Sequence
    » Timing Setup Hardware Unit Starting Flow
    » Path Pattern Program to PG
    » Read Control Data
Test Program / Test Flow (Cont. )

» Call PBDATA
» Timing guardband
» Setting Category and Sort Table
  – Start Program
    » Measure DC
    » Measure AC
    » Functional Test

• Pattern program
  – Edit ALPG micro-code to process Test Pattern

• Socket program
  – Parallel Test Setup
Items to Test for Memory IC

- DC Parametric Test
  Measure IC’s DC Voltage or current

- AC Parametric Test
  Measure IC’s AC Timing for Specification

- Functional Test
  Verify IC’s operation functions
DC Parametric Test

1. Open/Short Test (Contact Test)

   a. Signal Pin Open/Short Test

   - Test Module
     - Driver
     - ISVM
     - Provide current – 100uA
     - Expectation -0.6 ~ -0.8V
     - Signal pins
       /RAS, /CAS, /WE,
       /OE, A0 ~ A9, I/O1 ~ 4

   - DUT
     - VSS
DC Parametric Test (Cont.)

Program Example

;OPEN/SHORT TEST (SINGAL PINS)

PCON= 0 ; 10uF Bypass Capacitor is disconnected
VCON= 1 (or VSI) ; The Relay of PPS is disconnected
LCON= 0 ; Power Supply of Load Module is disconnected
ISVM= -100UA,R800UA, M8V, 1V, -5V
LIMIT DC=-0.0IV, -2V
TEST 10
MEAS/T DC(pin number)
b. VCC Pin Open/Short Test

;OPEN/SHORT TEST (VCC PINs)
VCON= I ; The Relay of PPS is disconnected
VS1=VSMV, -1V, R10V
LIMIT VS1=-0.3V, -0.7V
TEST 20
MEAS VS1
2. Standby ICC Current Test

Test Status

/RAS : High level,  /CAS : High level  I/O pins : Open,
10uF C : OFF,  Limit : 2mA

Test Module

PPS1

Guard
Sense
Force

CPS1

PBVCC

VCC

DUT

0.1uF
10uF
DC Parametric Test (Cont.)

Program Example

; STANDBY CURRENT ICC(ICC2)
PCON=0 ; 10uF Capacitor is disconnected
VCON=0 ; The relay of PPS1 is connected
LCON=0 ; Power Supply of Load Module is disconnected
TIMEI?MS: VSI
TIME2?MS: INI

;*****************************Power Supply Setting & Pin Condition Setting
VS1=5.5V, R8V, M400MA ; Vcc maximum value
LIMIT VS1= 1MA, 0 ; Maximum value of ICC2
INI=5.3V, OV ; CMOS interface (High level = VCC-0.2V)
RAS=IN1, FIXH ; /RAS is high level
CAS=IN1, FIXH ; /CAS is high level
ADR=IN1, FIXH ; Address Pins Level is "don't care"
WE=IN1, FIXH ; /WE level is "don't care"
OE=INIJIXH ; /OE level is "don't care"
IO=OPEN

;************************* Test Item & Measure Start
SRON ; Sequential Reference On happens
WAIT TIME 1MS ; Wait until Vcc Current becomes stable
TEST 100
MEAS VS1 ; ICC2 value is measured
DC Parametric Test (Cont.)

3. Operating ICC Current Test

Test Status

/RAS : As SPEC, /CAS : As SPEC
10uF C : ON, Limit : 2mA
I/O pins : Open,

Test Module

![Diagram of test module with components labeled as follows:
- Guard
- Sense
- Force
- CPS1
- PBVCC
- VCC
- DUT
- 0.1uF
- 10uF capacitor
]
DC Parametric Test (Cont.)

Program Example

; OPERATING CURRENT ICC(ICC3)
; *************************** pm Condition Setting
ADRX=IN1, FIXL
RASX=IN1, /RZO,BCLK4,CCLK4,<CO> ; /RAS Signal Definition
CASX=IN1, /RZO,BCLK5,CCLK5,<C1> ; /CAS Signal Definition
WE=IN1,FIXL
OE=IN1,FIXH
IO=OPEN

; *************************** Power Supply Setting, PG Start & Test Item Set
PCON=1 ; 10uF Bypass Capacitor is connected
VSI=5.5V,R8V,M400MA,200MA,-200MA ; Vcc maximum value
LIMIT VS1=100MA,0 ; Maximum value of ICC1
REG MPAT PC=#***
SEND MPAT filename ; Send the patterp program to ALPG
START MPAT * ; ALPG start to run
WAIT TIME 1MS ; Wait until Vcc Current becomes stable
TEST 120
MEAS VS I ; ICC I value is measured
SROF& STOP MPAT
DC Parametric Test (Cont.)

4. Current Leakage Test

a. ILIL (Input Leakage / Input Low)

Test Status

Vcc : 5.5V, 10uF C : OFF, Target input pin : 0V
The other input pins : 7V, I/O pins : Open, Limit : -10 ~ 10uA

Diagram:

- 7V
- Target pin
- VSIM=0V, R2V, M8UA
b. ILIH (Input Leakage / Input High)

Test Status

Vcc : 5.5V, 10uF C : OFF, Target input pin : 7V
The other input pins : 0V, I/O pins : Open, Limit : -10 ~ 10uA
DC Parametric Test (Cont.)

Program Example

; INPUT LEAKAGB CURRENT TEST
VSI=5.5V
INI=7V,OV
10=OPEN
VSIM=0V,R8V,M80UA,+112UA,-112UA ;Low level for a target input pin
LIMIT DC=IOUA,-IOUA
INP=IN1,FIXH ;High level for other input pin
TEST 140
MEAS DC(INP) ;ILIL is measured
VSIM=7V,R8V,M80UA,+112UA,-112UA ;High level for a target input pin
INP=IN1, FIXL ;Low level for other input pin
TEST 150
MEAS DC(INP) ;ILIH is measured
AC Parametric Test

Example: $T_{\text{CAC}}$ Test
Example: $T_{CAC}$ Test

$T_{CAC} = \text{STRB1} - \text{/CAS delay}$
AC Parametric Test (Cont.)

;TCAC MEASUREMENT
DIM ARG(11) ;Elcvcn array variable arc required for the TMEAS utility.

;*********************Voltage Setting
VSI=5.5V
OUTI=2.4V,0.8V
IN1=3V,OV

;********************* Timing Edge Setting
RATE=260NS
ACLK1=30NS & BCLK1=45NS & CCLK1=70NS
ACLK2=75NS & BCLK2=80NS & CCLK2=115NS
ACLK3=0NS & BCLK3=80NS & CCLK3=115NS
ACLK4=0NS & BCLK4=50NS & CCLK4=190NS
ACLK5=0NS & BCLK5=85NS & CCLK5=190NS
ACLK6=0NS & BCLK6=50NS & CCLK6=190NS
ACLK7=0NS & BCLK7=80NS & CCLK7=115NS
DREL1=80NS & DRET1=115NS
STRB1=120NS
SELECT DCLK ACLK1, BCLK1, CCLK1
AC Parametric Test (Cont.)

;************************Pin Condition Setting
PADR=IN1,XOR, ACLK1, BCLK1, CCLK1 ,SDM,<X0-9,Y0-9>
PRAS IN1, /RZ0, BCLK4, CCLK4,<CO>
PCAS =IN1, /RZ0, BCLK5 ,CLK5,<Cl>
PWE = IN1,/RZ0, BCLK7, CCLK7,<WT>
POE = IN1,/RZ0,BCLK6,CCLK6,<RD>
PIO IN1, XOR,ACLK3, BCLK3, DRERZ, IOC, OUT1, STRB1, LOD,<D0-3>

;*************************parameter Setting
ARG(1) =0NS ;Start value of ARG(3)'s unit
ARG(2) =120NS ;Stop value of ARG(3)'s unit.
ARG(3) =21 ;Unit number (21; STRBI).
ARG(6) =1 ;Timing set number 1; TS!
ARG(7) =0 ;Start PC value of ALPG.
ARG(8) =0 ;Tracking unit number.
ARG(9) =0 ;Tracking value for ARG(8).
ARG(10) =0 ;Timing set number of the tracking unit defined by ARG(8)
ARG(11) =1 ;DUT number.

;*************************Test Item Set & Call Utility Function
REGMPATPC=#0
SEND MPAT filename
TEST 200
ASM TMEAS(ARG) ;TCAC is measured.
Functional Test

1. Gross function Test
   - Read Cycle Test
   - Write Cycle Test
   - Fast Page Mode / EDO Mode Check
   - March Column / March Row

2. Special Pattern Test
   - Checkboard Pattern
   - Butterfly Pattern
   - Diagonals Pattern
   - Moving Inversion Pattern