Chapter 4. Field Effect Transistors (FETs)

Unipolar Device

(a) Perspective view
(b) Cross section

Nmos Transistor
1965 - 1990s
L ~ 1 - 10 µm
W ~ 2 - 500 µm

Today: Intel 0.065 µm = 65 nm

2010

Cross-section

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

p-type substrate

transistor
An NMOS transistor with $V_{gs} > V_t$ and with a small $V_{ds}$ applied.

\[ V_{gs} > 0, \quad V_{gs} = V_t \]

Concept of

$V_t = $ Threshold Voltage

Fig. 5.3
Figure 5.6  \( I_D \) versus \( V_{DS} \) for an enhancement-type NMOS transistor (\( V_{GS} > V_t \)).

\[ V_{GS} = V_{DS} \]

\[ V_{DS} = V_{G} - V_{T} \]

\[ V_{DS} > V_{T} \]

**Curves bends because the channel resistance increases with \( V_{DS} \)**

Almost a straight line with slope proportional to \((V_{GS} - V_{T})\)

**Current saturates because the channel is pinched off at the drain end, and \( V_{DS} \) no longer affects the channel.**

\[ V_{GS} > V_{T} \]

\[ V_{DS, sat} = V_{GS} - V_{T} \]

\[ V_{DS} \]

Overdrive voltage

\[ V_{G} - V_{T} = V_{0V} \]
Terminal voltages and regions of operation of the enhancement N-channel MOSFETs.

- **Gate:**
  - **Saturation Mode:** $V_{GT}$
  - **Drain**
  - **Triode or Linear Mode:** $V_{TD}$

**Important:**

Very useful diagram! Know how to use it!

- **$V_{DS}$ vs. $V_{DS}$**
  - **Cutoff**
  - **Saturation**
  - **Triode Regime**

For N-channel enhancement mode device:

$V_{T} > 0$
In Triode Mode: \( V_{DS} \leq V_{GS} - V_t \) (Solid State Electronics I)
\[
i_D = \frac{k'_n}{L} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]
\]
with \( k'_n = \frac{\mu_n C_Ox}{2} \) where \( [\mu_n] = \frac{C_m}{V_a} \)

In Saturation Mode: \( V_{DS} > (V_{GS} - V_t) \)
\[
i_D = \frac{1}{2} \frac{k'_n}{L} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2
\]

**FIGURE 4.11** (a) An n-channel enhancement-type MOSFET with \( v_{GS} \) and \( v_{DS} \) applied and with the normal directions of current flow indicated. (b) The \( i_D-v_{DS} \) characteristics for a device with \( k'_n (W/L) = 1.0 \text{ mA/V}^2 \).
CHAPTER 4 MOS FIELD-EFFECT TRANSISTORS (MOSFETs)

In saturation mode
\[ I_{DS} = \frac{1}{2} k \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]

Quadratic Dependence

Note that
\[ V_{DS} \geq V_{GS} - V_T \]

cutoff

FIGURE 4.12 The \( I_D-V_{GS} \) characteristic for an enhancement-type NMOS transistor in saturation \( (V_T = 1 \text{ V}, \ k_n' W/L = 1.0 \text{ mA/V}^2) \).

\[ i_C = 0 \quad \text{for} \quad \frac{V_{DS}}{W} \gg V_T \]

For \( \frac{V_{DS}}{W} \gg V_T \)

DC Model for SPICE

\( \text{Large-signal equivalent circuit} \)
\[ i_D = \frac{1}{2} k_n' W \frac{v_{GS} - V_t}{L} (1 + \lambda v_{DS}) \]

**FIGURE 4.16** Effect of \( v_{DS} \) on \( i_D \) in the saturation region. The MOSFET parameter \( V_a \), depends on the process technology and, for a given process, is proportional to the channel length \( L \).

\[ -V_A = -1/\lambda \]

**DIAGRAM**

**DC Model for SPICE**

\[ r_o = \left[ \frac{\partial i_D}{\partial v_{DS}} \right]_{v_{GS} \text{ constant}} \]

\[ r_o = \left[ \frac{\lambda k_n' W}{2 L} (V_{GS} - V_t)^2 \right]^{-1} \]

**FIGURE 4.17** Large-signal equivalent circuit model of the \( n \)-channel MOSFET in saturation, incorporating the output resistance \( r_o \). The output resistance models the linear dependence of \( i_D \) on \( v_{DS} \) and is given by Eq. (4.22).
p-channel MOSFETs (enhancement mode)

Circuit symbol

\[ \text{arrow pointing towards gate} \]

\[ V_T < 0 \]

To induce channel \( V_{GS} \leq V_T \)

\[ \text{both negative} \]

**Drain**

\[ i_D = k_p \left( \frac{W}{L} \right) \left( V_{GS} - V_T \right)^2 N_{DS} \left( \frac{1}{2} N_{DS}^2 \right) \]

\[ k_p = \mu_p C_{ox} \]

\[ \mu_p = \frac{1}{2} \mu_n \] Typically

**Saturation** \( N_{DS} \leq N_{GS} - V_T \)

\[ i_D = \frac{1}{2} k_p \left( \frac{W}{L} \right) \left( V_{GS} - V_T \right)^2 \left( 1 + 2 N_{DS} \right) \]

Same equations as for n-channel

except \( k_m \rightarrow k_p \)

only if early effect is negligible.
The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode and p-channel saturation regimes.

This diagram is a mirror image of a diagram for NMOS enhancement device.
The image contains a diagram of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) with various states and equations. Here is a detailed description:

**P-MOS Enhancement (V_T < 0):**
- Gate and Drain are tied together and V_DS > V_T, the device is in saturation.
- Source → V_T → Triode → Drain

**N-MOS Enhancement (V_T > 0):**
- Gate and Drain are tied together and V_DS < V_T, the device is in depletion.
- Source → V_T → Triode → Drain

**Saturation:**
- N_DS = N_D - V_T

**P-MOS Depletion (V_T > 0):**
- Gate and Drain are tied together and V_DS < V_T, the device is in saturation.
- Source → V_T → Triode → Drain

**N-MOS Depletion (V_T < 0):**
- Gate and Drain are tied together and V_DS > V_T, the device is in saturation.
- Source → V_T → Triode → Drain

Equations:
- For P-MOS:
  \[ I_D = k^1 \left( \frac{V_T}{V_T} \right) \left( \frac{V_T}{V_T} \right)^2 \]
- For N-MOS:
  \[ I_D = \frac{1}{2} k^1 \left( \frac{V_T}{V_T} \right)^2 \]

**Output Characteristics:**
- Triode: \( k^m = \mu_m C_{ox}, \quad k_p = \mu_p C_{ox} \)
Ex. 4.1

\[ L = 0.4 \text{um} \]
\[ t_{ox} = 8 \text{nm} \]
\[ \mu_m = 450 \text{ cm}^2/\text{V.s} \]
\[ V_T = 0.7 \text{V} \]

Given N-channel parameters

\[ C_{ox} = \frac{E_{ox}}{t_{ox}} \]
\[ k'_m \]
\[ \frac{C_{ox}}{E_{ox}} \]

\[ k'_m = \mu_m C_{ox} = 450 \text{ cm}^2/\text{V.s} \times 4.32 \text{ (F/cm}^2) = 194 \text{ mA/V}^2 \]
\[ C_{ox} = \frac{E_{ox}}{t_{ox}} \text{ (capacitance per unit area of gate)} = 4.32 \times 10^{-3} \text{ F/m}^2 \]
\[ E_{ox} = 3.9 \varepsilon_0 = 3.9 \times 8.85 \times 10^{-12} \text{ F/m} \]

For a N-channel MOSFET with \( W/L = 8 \text{ um} / 0.8 \text{ um} \), what are the values of \( V_{GS} \) and \( V_{DS, \text{min}} \) needed to operate the transistor in saturation region with a DC current of 100 \( \mu \text{A} = 0.1 \text{ mA} \)?

Saturation:
\[ I_D = \frac{1}{2} k'_m \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]
\[ 100 = \frac{1}{2} 194 \left( \frac{8}{0.8} \right) (V_{GS} - 0.7)^2 \]
\[ \rightarrow V_{GS} - 0.7 = 0.32 \text{V} \]
\[ \rightarrow V_{GS} = 1.02 \text{V} \]

\[ V_{DS, \text{min}} = V_{GS} - V_T = 0.32 \text{V} \]

Why not \( V_{GS} = 0.7 - 0.32 \)?

For what value of \( V_{GS} \) will the device operate as a 1kΩ resistor for small \( V_{DS} \)?

In triode mode (small \( V_{PS} \));
\[ I_D = \frac{1}{2} k'_m \left( \frac{W}{L} \right) (V_{GS} - V_T) V_{DS} \]

From 167
\[ I_D = \left[ \frac{k'_m}{2} \left( \frac{W}{L} \right) (V_{GS} - V_T) \right] \]
\[ \Rightarrow I_{DS} = 100 \mu A = 194 \times 10^{-6} \times 10 (V_{GS} - 0.7) \]
\[ \rightarrow V_{GS} = 1.22 \text{V} \]
Design this circuit so that:

\[ I_D = 0.4 \, \text{mA} \]
\[ V_D = 0.5 \, \text{V} \]

Given:
\[ V_T = 0.7 \, \text{V} \]
\[ \mu_m C_0 x = 100 \, \mu \text{A/V}^2 \]
\[ L = 1 \, \mu \text{m} \]
\[ W = 32 \, \mu \text{m} \]

\[ \Rightarrow R_s, R_D \]

Reflect channel-length modulation \( \mu = 0 \)

\[ V_D > V_G \Rightarrow \text{N沟道 operating in saturation mode (see p.173)} \]

\[ I_D = \frac{1}{2} \mu m C_0 \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]

Calc:
\[ V_{GS} = \text{gate-source voltage} = V_{GS} - V_T \]
\[ I_D = 0.4 \, \text{mA} = 400 \, \mu \text{A}, \quad \mu m C_0 x = 100 \, \mu \text{A/V}^2, \quad \frac{W}{L} = 32 \]

\[ \Rightarrow 400 = \frac{1}{2} \times 100 \times \frac{32}{1} \times V_{GS}^2 \]

\[ \Rightarrow V_{GS} = 0.5 \, \text{V} = V_{GS} - V_T \]

\[ \Rightarrow V_{DS} = V_T + V_{GS} = 0.7 + 0.5 = 1.2 \, \text{V} \rightarrow V_S = -1.2 \, \text{V} \quad \text{since } V_G = 0 \]

\[ \Rightarrow V_{DS} = V_T + V_{OU} = 1.2 \, \text{V} \rightarrow V_{DS} = 1.2 \, \text{V} \]

\[ \text{Needed} \quad R_s = \frac{V_S - V_{DS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \, \text{k}\Omega \]

For \( V_D = 0.5 \), we must select:

\[ R_D = \frac{V_{PD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \, \text{k}\Omega \]
Example 4.3 p. 264

Design the circuit below to have \( I_D = 80 \mu A \) = 0.08 mA

Which \( R \) is needed? What is the value of \( V_D \)?

Given:
\[ V_T = 0.6V, \quad \mu \approx u m C_X = 20 \mu A/V^2 \]
\[ L = 0.8 \mu m, \quad W = 4 \mu m; \quad \text{Assume} \quad \lambda = 0. \]

Here \( N_D \) forced equal to \( N_G \) \( \rightarrow \) Saturation Mode automatically.

\[ I_D = \frac{1}{2} \mu \approx u m C_X \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]

\[ \Delta V_{OV} = V_{GS} - V_T \]

\[ V_{OV} = 0.4 \text{V} \Rightarrow V_{GS} = V_T + V_{OV} = 0.6 + 0.4 = 1 \text{V} \]

\[ \Rightarrow V_D = V_G = 1 \text{V} \]

\[ R = \frac{V_{PD} - V_P}{I_P} = \frac{3-1}{0.080} = 25 \text{ k}\Omega \]
Example 4.5 p 266

Determine voltage in all nodes and branches.

\[ V_T = 1V \]

\[ I_m \left( \frac{W}{L} \right) = 1mA/V^2 \]

Assume \( \lambda = 0 \).

**Exact**

\[ I_G = 0 \rightarrow V_G = +5V \]

(voltage divider of \( R_{G2} \) & \( R_{G1} \))

large positive voltage \( \rightarrow \) NPN is on!

Question? Triode or Saturation mode?

Assume Saturation & check if everything falls into place.

\[ T_S = 6I_D \quad \text{(CAREFUL)} \]

\[ \Rightarrow V_{GS} = 5 - 6I_D = V_T - I_D \frac{V_T}{I_D} \]

\[ \Rightarrow I_D = \frac{1}{2} \frac{1}{I_m} \left( \frac{V_T}{I_D} \right) \left( 5 - 6I_D - 1 \right)^2 = \frac{1}{2} \times 1 \times (4 - 6I_D)^2 \]

\[ 4 - 6I_D = 2I_D \quad [I_D \text{ in } mA] \]

\[ 36I_D^2 - 48I_D + 16 = 2I_D \]

\[ 36I_D^2 - 50I_D + 16 = 0 \]

\[ \Rightarrow 18I_D^2 - 25I_D + 8 = 0 \]

\[ \Rightarrow I_D1 = 0.89mA \]

\[ \Rightarrow I_D2 = 0.5mA \]

With \( I_{D1} \)

\[ T_S = 6 \times 0.89 = 5.34 \]

\[ T_S > V_G > V_G \quad \text{invalid! NOT PHYSICALLY ACCEPTABLE (CUT OFF MODE)} \]

\[ I_{D2} = 0.5mA \rightarrow V_S = 0.5 \times 6 = 3V \]

\[ V_{GS} = 2V \]

\[ V_D = 10 - 6 \times 0.5 = +7V \]

\[ \Rightarrow T_{DS} > V_S - V_T \]

Saturation Indeed!
Example 4.7 p.269

Nmos & Pmos are matched i.e.

Assume \( I = 0 \)

Find \( I_{DN}, I_{DP}, V_0 \), for \( V_I = 0V, +2.5V, -2.5V \)

If \( V_I = 0 \).

\( |V_{GS}| = 2.5V \) for both devices

\( |V_{GS}| > V_F = 1V \) Both devices conduct!

\[
I_D = \frac{1}{2} \frac{k}{L} (V_{GS} - V_T)^2
\]

or

\[
I_D = \frac{k}{L} (V_{GS} - V_T + V_T^2 - \frac{1}{2} V_{DS}^2)
\]

Same for both devices since they are matched.

\( N_I = 0 \)

\( I_D \) same for both devices \( \rightarrow N_0 = 0 \)

So \( Q_n, Q_p \) operate with \( V_{DG} = 0 \) \( \rightarrow \) Saturation mode. Why?

\[
-2.5V \quad -1.0V \quad +2.5V
\]

\( V_{DS} = V_{GS} V_T \)

\( N_D = \frac{V_T - V_{DS}}{V_{DS}} \)

\( N_{PDS} \)

\( I_{DP} = I_{DN} = \frac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{mA} \)
\[ V_T = +2.5 \text{V} \]

Qp has \( V_{GS} = 0 \) \( \rightarrow \) Qp is cut off

\[ +2.5 \text{V} \quad \overset{N_G}{\longrightarrow} \quad \overset{N_D}{\longrightarrow} \quad \overset{N_0}{\longrightarrow} \]

Qn

\[ -2.5 \text{V} \]

\( N_0 \) is negative = \( N_D \) of MOSFET transistor

\[ V_{GD} > V_T \text{ or } V_{GS} - V_{DS} > V_T \text{ or } V_{DS} < V_{GS} - V_T \]

\[ \rightarrow \text{Triode mode of operation} \]

Assume \( V_{DS} \) small for simplicity \( \rightarrow \) neglect

\[ I_{DN} = I_{m0} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) \frac{V_{DS}}{V_T} - \frac{1}{2} \frac{V_{DS}^2}{V_T^2} \right] \]

\[ I_{DN} = \frac{1}{8} \left[ (2.5 - (-2.5)) - 1 \right] \left( \frac{N_0}{2.5} \right) \]

Also \( I_{DN} (\mu A) = \frac{0 - N_0}{10(\mu A)} \)

\[ \rightarrow I_{DN} = 0.244 \mu A \quad N_0 = -2.44 \text{V} \quad \text{small} \]

\[ \rightarrow V_{DS} = -2.44 - (-2.5) = 0.06 \text{V}, \text{as assumed!} \]

\[ \frac{F_{O2}}{V_I} = -2.5 \text{V} \]

Qn will be off \( \rightarrow I_{DN} = 0 \)

Qp will be operating in triode

\[ I_{DP} = 2.44 \mu A \]

\[ N_0 = 2.44 \text{V} \]

Try to show this yourself.

\[ \text{We have an inverter!} \]
Depletion type MOSFET

- Electrons are already in channel for this device without putting potential on terminals.
- $V_{GS}$ can be swept negative!
  If too negative, electron channel disappears → The threshold voltage for this device is negative!
- $V_{GS}$ can still be swept positive for this device.

Circuit Symbol

**MOS-Depletion**

**Tricdle**

$$I_D = k_m \left( \frac{W}{L} \right) \left[ (V_{GS} - V_E) \frac{V_{DS}}{2} - \frac{1}{2} V_{DS}^2 \right]$$

**Saturation**

$$I_D = \frac{1}{2} k_m \left( \frac{W}{L} \right) (V_{GS} - V_E)^2$$
The current-voltage characteristics of a depletion-type $n$-channel MOSFET for which $V_T = -4$ V and $k_n^d (W/L) = 2$ mA/V$^2$: (a) transistor with current and voltage polarities indicated; (b) the $i_D-v_{DS}$ characteristics; (c) the $i_D-v_{GS}$ characteristic in saturation.
Equations for \( I_D \) for triode mode and saturation modes of operation are the same.

They can also be swept positive and negative.

\( V_T \) is POSITIVE.

**FIGURE 4.62** Sketches of the \( i_D - V_{GS} \) characteristics for MOSFETs of enhancement and depletion types, of both polarities (operating in saturation). Note that the characteristic curves intersect the \( V_{GS} \) axis at \( V_T \). Also note that for generality somewhat different values of \( |V| \) are shown for \( n \)-channel and \( p \)-channel devices.
FIGURE 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate $n$-type region, known as an $n$ well. Another arrangement is also possible in which an $n$-type body is used and the $n$ device is formed in a $p$ well. Not shown are the connections made to the $p$-type body and to the $n$ well; the latter functions as the body terminal for the $p$-channel device.
**BIASING DEPLETION MODE**

**PnFETs**

\[ V_F = -2 \text{ V} \]

**Depletion N\text{MOS}$$

\[ k_m \left( \frac{W}{L} \right) = 4 \text{ mA/V}^2 \]

What is the value of \( I_{DSS} \)?

\( I_{DSS} = I_D \) when \( V_{GS} = 0 \)

\[ I_D = \frac{1}{2} k_m \frac{W}{L} \left( V_{GS} - V_T \right)^2 \]

\( V_D = 5 \text{ V} \)

\( V_{GS} = 2 \text{ V} \)

\( V_T = 2 \text{ V} \)

\( V_S ? \)

\[ I_D = 2 \text{ mA} = 2 \text{ mA} \left( V_{GS} + 2 \right)^2 \]

\[ \left( V_{GS} + 2 \right)^2 = 1 \]

\[ V_{GS1} = -1 \text{ V} \]

\( \text{or} \quad V_{GS2} = -3 \text{ V} \)

\( V_S = +1 \text{ V} \)

Ex. 4.51 P. 351

\[ I_m = 2 \text{ mA} \]

\( I = 0 \) calculate \( V_T \)

\[ V_{D} > V_{GS} - V_T \rightarrow \text{Sol.} \]

So, \( V_D > V_{GS} - V_T \rightarrow \text{Sol.} \)

\[ V_{GS} = -1 \text{ V} \]

\[ \rightarrow V_S = +1 \text{ V} \]

\[ \text{No! Cut off} \]