Example Altera Design Report (Neena Sharma, 08/20/12: 1 Protocol bridge I2C master implementation [excerpts])

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Analysis & Synthesis Summary

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Analysis & Synthesis Status Successful - Fri Aug 03 10:34:01 2012

 Quartus II Version 10.0 Build 218 06/27/2010 SJ Web Edition

 Revision Name I2C\_master

 Top-level Entity Name I2C\_master

 Family Cyclone IV E

 Total logic elements 77

 Total combinational functions 77

 Dedicated logic registers 34

 Total registers 34

 Total pins 38

 Total virtual pins 0

 Total memory bits 0

 Embedded Multiplier 9-bit elements 0

 Total PLLs 0

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 Fitter Summary

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 Fitter Status Successful - Fri Aug 03 10:34:52 2012

 Quartus II Version 10.0 Build 218 06/27/2010 SJ Web Edition

 Revision Name I2C\_master

 Top-level Entity Name I2C\_master

 Family Cyclone IV E

 Device EP4CE115F29C7

 Timing Models Final

 Total logic elements 77 / 114,480 ( < 1 % )

 Total combinational functions 77 / 114,480 ( < 1 % )

 Dedicated logic registers 34 / 114,480 ( < 1 % )

 Total registers 34

 Total pins 38 / 529 ( 7 % )

 Total virtual pins 0

 Total memory bits 0 / 3,981,312 ( 0 % )

 Embedded Multiplier 9-bit elements 0 / 532 ( 0 % )

 Total PLLs 0 / 4 ( 0 % )

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 Operating Settings and Conditions

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Nominal Core Voltage 1.20 V

Low Junction Temperature 0 °C

High Junction Temperature 85 °C

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Clocks

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Clock Name Type Period Frequency Rise Fall

clk Base 1.000 1000.0 MHz 0.000 0.500