The Fabrication and Characterization of GaAs n-MESFET

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1. Introduction and Theory

1.1 Purpose of project

The students will learn the engineering and technology of III-V semiconductor device fabrication, fabrication process design and device and process characterization.

By completely finishing the whole series of lab sessions in this project for GaAs MESFET technology, it is highly helpful for us to improve our skills in practicing on the complete fabrication process for GaAs MESFET, including different layers of mask designing with AUTOCAD, resist application, development and processing, silicon nitride deposition and etching (wet and RIE), photolithography, Ion implantation and subsequent rapid thermal annealing, metallization (ohmic contact and Schottky contact) and its liftoff process. Finally, test structure measurements, MESFET characterization and evaluation of finished devices, as well as the related discuss to experimental results will help us improve our understanding on fundamental physics of micro fabrication and equip us acquired analytical skills in research, dissertation work or future job.
1.2 The introduction to GaAs MESFET

The technology of metal–semiconductor field effect transistor (MESFET) based on GaAs substrate has undergone a rapid development in recent years. The use of GaAs substrates for IC circuits offers some outstanding advantages over the traditional Si substrate, especially in the area of high frequency and high speed microwave circuits. Its application extends to low noise preamplifiers and linear amplifiers, oscillators and mixers in communication networks due to some of its outstanding physical properties, such as high cutoff frequency (more than 10 GHz for 1 μm gate length) and high electron mobility. Furthermore, GaAs circuits are suited for optoelectronic applications due to its direct-bandgap property which can be grown with semi-insulating bulk conductivity. At the same time, the commercial availability of improved technology, such as, dry etching, plasma-enhanced chemical vapor deposition, submicrometer optical lithography, and rapid thermal annealing equipment have made the fabrication for advanced GaAs MESFET simpler and lower cost.

In the operation of a MESFET, the electrical conduction between the source and drain is modulated by a bias applied to the gate. The Schottky barrier formed by metal-semiconductor junction makes the gate isolated to channel. Thus, by controlling the doping level of the channel it is possible to obtain enhancement- or depletion-mode transistors. The switching characteristics of such digital inverters made from GaAs MESFET’s are comparable, even much superior than those the Si-based digital inverters. The typical intrinsic time delay for such kind of inverters can be lower than 100 ps for 1-μm gate length devices.
1.3 The properties of GaAs

Perhaps the primary benefit of GaAs comes from its electron-dynamic properties. In equivalently doped n-type GaAs and silicon, the effective mass of the electrons in GaAs is far less than that in Si. This means that the electrons in GaAs are accelerated to higher velocities and therefore transverse the transistor channel in less time. This improvement in electron mobility is the fundamental property that enables higher frequencies of faster switching speed.

GaAs is a III-V compound semiconductor composed of element gallium (Ga) from column III and the element arsenic (As) from column V of the periodic table of the elements. GaAs was first created by Goldschmidt and reported in 1929, but the first reported electronic properties of III-V compounds as semiconductors did not appear until 1952.

The GaAs crystal is composed of composed of two sub lattices, each face centered cubic (fcc) and offset with respect to each other by half the diagonal of the fcc cube. This crystal configuration is known as cubic sphalerite or zinc blende. The basic properties of GaAs at 300K are as follows,

<table>
<thead>
<tr>
<th>Crystal structure</th>
<th>Zinc Blende</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group of symmetry</td>
<td>$Td^2-F43m$</td>
</tr>
<tr>
<td>Number of atoms in 1 cm$^3$</td>
<td>$4.42\times10^{22}$</td>
</tr>
<tr>
<td>de Broglie electron wavelength</td>
<td>240 $\text{Å}$</td>
</tr>
<tr>
<td>Debye temperature</td>
<td>360 $K$</td>
</tr>
<tr>
<td>Density</td>
<td>5.32 g cm$^{-3}$</td>
</tr>
<tr>
<td>Dielectric constant (static)</td>
<td>12.9</td>
</tr>
<tr>
<td>Dielectric constant (high frequency)</td>
<td>10.89</td>
</tr>
<tr>
<td>Effective electron mass $m_e$</td>
<td>$0.063m_o$</td>
</tr>
</tbody>
</table>
GaAs is a direct band gap semiconductor, which means that the minimum of the conduction band is directly over the maximum of the valence band (Fig. 1.2). Transitions between the valence band and the conduction band require only a change in energy, and no change in momentum, unlike the indirect band-gap semiconductor such as silicon. This property makes GaAs a very useful material for the manufacture of light-emitting diodes and semiconductor lasers, since a photon is emitted when an electron changes energy level from the conduction band to valence band.

And the crystal structure and energy band structure of GaAs are shown in the following figures,
1.4 Device description

In recent years the field of high-speed transistors has greatly expanded to include devices made of sophisticated heterostructures. However, the most prevalent and well-developed high-speed transistors remain those in which carriers flow through a homogeneous semiconductor layer and are controlled by the influence of the voltage placed on a control electrode. Although the homogeneous field-effect transistors (FETs) don’t take advantages of the special properties of heterojunctions, many offer greater simplicity and ease of fabrication because they don’t depend as critically upon the precise fabrication of thin layers and sharp interfaces. FETs are unipolar or majority-carrier devices and don’t exhibit the minority-carrier effects that can hamper the speed and thermal stability of bipolar transistors. Homogeneous FETs offer high performance at low cost and have established a proven track record of utility and reliability in important systems applications.

The metal-semiconductor field-effect transistor (MESFET) was proposed by Mead in 1966 and subsequently fabricated by Hooper and Lehrer using a GaAs epitaxial layer on semi-insulating GaAs substrate. The operation of a MESFET is identical to that of a JFET (junction field-effect transistor). In MESFET,
however, a metal-semiconductor rectifying contact instead of a p-n junction is used for the gate electrode. The MESFET offers certain processing and performance advantages, such as low-temperature formation of the metal-semiconductor barrier (as compared to a p-n junction made by diffusion or grown processes), low resistance and low IR drop along the channel width, and good heat dissipation for power devices (the rectifying contact can also serve as an efficient thermal contact to heat sink). The cross section of the GaAs MESFET is shown in Fig. 1.2

![Schematic diagram of a MESFET.](image)

Recently, the GaAs MESFET is interested by people because of high speed microwave circuits, simple fabrication process (no epitaxy) and low cost. The electron mobility in GaAs channel is much higher than in Silicon channel. High electron mobility in GaAs channel gives high drain current $I_D$ and transconductance because $g_m$

$$I_D \sim n_{\text{channel}} \mu_n \frac{W}{L_g}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \sim n_{\text{channel}} \mu_n \frac{W}{L_g}$$

High electron mobility in GaAs channel also gives short transit time and high speed because channel transit time $\tau$
\[ \tau \approx \frac{L_s}{v_n} \sim \frac{L_s}{\mu_n} \]

and cutoff frequency \( f_T \)

\[ f_T = \frac{g_m}{2\pi C_G} \sim \frac{N_D(\text{channel})\mu_n}{I_s^2} \]

The following two figures show the advantages of GaAs MESFET over Si NMOS in current-drive capability and cutoff frequency.

Fig.1.3 current-drive capability and cutoff frequency

### 1.5 Ohmic Contact

The purpose of an ohmic contact on a semiconductor is to allow electrical current to flow into or out of the semiconductor. The contact should have a linear I - V characteristic, be stable over time and temperature, and contribute as little (parasitic) resistance as possible. From above equation we can find that the depletion layer \( W \), is inversely proportional to the square root of \( N_d \), the doping concentration of the semiconductor. The width of the depletion region decreases as the doping concentration increases; thus the probability of tunneling through
barrier increases. The more the electrons that is able to tunnel through the barrier, the more current flows from semiconductor to the metal, creating an ohmic contact. The condition for the source and drain regions is that the more heavily doping the region the better the ohmic contact the junction makes. The system just described is called a tunneling barrier contact, which is shown on Fig. 1.4

![Energy band diagram of a n+ doped semiconductor to metal junction](image)

Fig.1.4 Energy band diagram of a n+ doped semiconductor to metal junction, with electron tunneling through the barrier

There are also ideal non-rectifying barrier contacts, which are realized when the metal work function is smaller than the semiconductor work function. In this case electrons flow from the metal into the semiconductor to achieve thermal equilibrium, bending the Ec and Ev bands down into the junction, therefore allowing current to flow in both directions.

1.6 Schottky Barrier
The Schottky barrier gate is one of the two most important elements of many GaAs devices; the other is an ohmic contact. The size and placement of the gate is critical to FET performance in both power and low noise FETs and in FETs
used in digital circuitry. Uniformity of device performance also requires reproducible size and placement of the gate [2].

The Schottky contact is formed when a metal and semiconductor are in intimate contact and the work function of the metal $\Phi_m$ is larger than the work function of the semiconductors. When there is contact, a potential barrier of height $\phi_m$ is formed between the metal and the semiconductor, which equals to the work function of the metal minus the electron affinity of the semiconductor ($\chi$).

A built-in potential $V_{bi}$ is created at a Schottky contact due to a misalignment in the Fermi energy of metal and the semiconductor. Typically, the work function of the metal is greater than that of an n-type semiconductor, and the semiconductor valence and conduction bands will bend upward at the interface in order to align the Fermi levels. The amount that the energy bands bend upwards at the interface is known as the built-in potential $V_{bi}$. The relation of these parameters is shown in Fig. 1.5.

Fig. 1.5 The energy band diagram of Schottky contact
The Schottky junction can be operated in the forward bias mode, and in reverse bias mode. In reverse bias mode, the junction barrier is increased from the semiconductor to the metal. In forward bias mode, the barrier from the semiconductor is reduced, allowing the majority carriers to shoot across from the semiconductor to the metal. The amount of increase and decrease in the barrier depends on the amount of bias voltage applied.

Two important characteristics are the depletion with $W$, given by:

$$W = \{2\varepsilon_S (V_{bi} + V_R) / qN_d \}^{1/2}$$

and the junction capacitance $C_{sc}$, given by:

$$C_{sc} = \{2qN_d\varepsilon_S / 2(V_{bi} + V_R) \}^{1/2}$$

Where:

- $\varepsilon_S$ : dielectric constant of the semiconductor.
- $N_d$ : dopant concentration in the channel (donor).
- $q$ : electron charge.
- $V_R$ : applied reverse bias.

Both of these Schottky parameters play an important role in determining the performance of the n-channel under reverse bias.
Chapter 2 Fabrication Overview and Process Design

The overall step-by-step MESFET fabrication processes are described here by referring each step to a particular Standard Operating Procedure (SOP) number. The fabrication process starts by inspection and cleaning of the wafer following specific procedures and ends at contact metallization and finally packaging, but only up to metallization processes are presented here. A number of theoretical calculations are also provided here to predict the device characteristics and the important parameters. The calculations of implant profile, sheet resistance, gate built-in potential, Pinchoff and Threshold voltage are done using the process parameters used in the laboratory. Finally, comparisons of the theoretical calculations with the simulation results are provided.

2.1 MESFET fabrication process

The overall MESFET fabrication processes are described below in a numbered fashion below. This schedule describes a four mask, double implant process for formation of GaAs MESFETs with implanted channels. The four mask levels are: 1. channel implant, 2. source/drain implant, 3. ohmic contact formation and 4. Schottky gate formation. The masks are all light field and positive resist is used throughout the process.

1. Initial wafer cleaning (SOP # 200).
2. Silicon nitride cap deposition by reactive sputtering (SOP # 210).
   i. cap thickness = 100 nm
3. Resist patterning for channel implant using positive resist (SOP # 120, 122, 123, 124B, 126 and 127)
   i. resist thickness = 1.6 µm
4. Silicon ion implantation of device channel regions (SOP # 202)
   i. maximum ion energy = 180 keV
   ii. ion species = Si⁺ (singly ionized)
   iii. dose = 5 x 10¹² /cm²
5. Shallow etching of silicon nitride for alignment registration purposes
6. in buffered HF solution and plasma etching (SOP # 210).
7. Resist stripping and ashing in oxygen plasma.
8. Resist patterning for source/drain implant using positive resist (SOP # 120, 122, 123, 124B, 126 and 127)
   i. Target resist thickness = 0.8 µm
9. Silicon ion implantation of device source and drain regions (SOP # 202)
   i. Maximum ion energy = 200 keV
ii. Ion species = Si\(^+\) (singly ionized)

iii. Dose > 1 \times 10^{13} /\text{cm}^2

10. Resist stripping and ashing in oxygen plasma.

11. Annealing of ion implants using rapid thermal annealing (SOP # 203).
   i. Maximum temperature = 850 °C
   ii. Ambient = forming gas
   iii. Time = 90 to 120 seconds

12. Resist patterning for ohmic contact formation (SOP # 120, 122, 123, 124B, 126 and 127).
   i. Target resist thickness = 0.8 \mu m

13. Silicon nitride etching for ohmic contacts.

14. CF\(_4\) plasma etching to semiconductor surface.

15. Final wet etch cleaning of exposed GaAs surface in 50 %HCl (SOP # 210).

16. Deposition of AuGe/Ni metal for ohmic contacts to source and drain using

17. E-beam evaporation and patterning by liftoff technique (SOP # 207 & 208).

18. Ohmic contact alloying by rapid thermal heating (SOP # 203).
   i. Maximum temperature = 475 – 500 °C
   ii. Ambient = forming gas
   iii. Time = 120 seconds

19. Resist patterning for nitride etch for Schottky gate formation (SOP # 120, 122, 123, 124B, 126 and 127).
   i. Target resist thickness = 1.6 \mu m

20. Silicon nitride etching for Schottky gate formation.

21. CF\(_4\) plasma etching to semiconductor surface.

22. Final wet etch cleaning of exposed GaAs surface in 50 %HCl (SOP # 210).

23. Aluminum metal deposition for Schottky gate formation using e-beam evaporation and patterning by liftoff technique (SOP # 207 & 208).

The basic fabrication process for constructing GaAs MESFETs uses a simple four-mask, double ion implantation process as shown in Figure 2.1.
This process begins with the preparation of the GaAs wafer which is usually selected to have a (100) surface, zero intentional doping and a very high resistivity (\( > 10^8 \text{ ohm-cm} \)) making it semi-insulating. This type of substrate is used to reduce parasitic effects.
capacitances and for device isolation. To prepare the substrate, the GaAs wafer is slightly etched to remove about 100 nm to remove surface oxide, contamination and damage from packaging and handling. A silicon nitride insulating layer is then deposited by reactive sputtering to a thickness of 100 nm. This capping layer protects the GaAs surface during the entire processing operation and helps to prevent loss of As from the surface by decomposition of the GaAs during high temperature processing.

The first masking step (mask #1) in the fabrication is the formation of the channel regions between the source and drain regions using a silicon ion implantation process. Since the GaAs substrate is semi-insulating, implantation of silicon ions is used to form a lightly doped but conducting, n-type region. The energy and dose for the silicon implantation is determined from the pinchoff voltage required for the MESFET. Positive resist is used to define the channel location (area of the wafer surface to be implanted) and implantation is done through the silicon nitride cap layer. After implantation, the silicon nitride is slightly etched (about 30 nm deep) in order to mark the wafer surface before the resist is removed for subsequent alignment of masks for the source and drain and gate regions. The resist is then stripped off the wafer leaving the nitride intact.

Formation of the source and drain regions for the MESFET is done in the next masking step (mask #2) in a similar fashion. Positive resist is again used to define the area of the implant and implantation is done through openings in the resist and through the silicon nitride cap layer. The energy and dose for the silicon implantation is now determined by the need for low resistance, ohmic source/drain regions contacting the ends of the channel. Higher doping levels are required (> $10^{18}$ /cm$^3$) to provide low resistance contacts and to form low resistance, ohmic metal-semiconductor contacts for contacting metal to the MESFET's source and drain regions. The resist is then removed (stripped) after the implant.

Since implantation produces severe damage to the semiconductor lattice, a thermal annealing step is needed after the implant to repair the damage and to activate the implanted species. After removal of the resist from the source/drain implant, the wafer is rapid thermally annealed at an elevated temperature for a brief period (seconds). The silicon nitride cap on the wafer during this process helps to control the decomposition of the GaAs surface which can occur by the preferential loss of As. This completes the formation of the active regions of the device.

Next, to make electrical contacts to the device's source and drain regions, resist is applied and patterned (mask # 3) and openings in the silicon nitride are etched down to the semiconductor surface over the source and drain regions. After patterning, the resist is treated in chlorobenzene to swell its top surface and produce an overhanging ledge at the top of the resist in the windows. The underlying silicon nitride is etched away in the windows to expose the underlying GaAs surface. The contact metal Au/Ge/Ni is then deposited, patterned and the excess metal removed (lifted off) by dissolving the resist in a solvent. This same lithography process and liftoff technique is also used to pattern the aluminum Schottky metal (mask #4) to form the gate electrode for the MESFET.

The MESFET's fabrication is now complete and the device is ready for testing and electrical characterization. The fabrication process outlined above is a basic one with a minimum of mask levels and processing. More sophisticated fabrication processes may
contain more mask levels, for example to define a second layer of metal for interconnection of devices. Over the course of this quarter, we will proceed systematically through this fabrication process by performing a set of process steps each week. The aim is to complete the device fabrication by the end of the eighth week so that electrical characterization of the devices and test structures can be done in the last two weeks.

2.2 Theoretical calculations of Implantation

Ion implantation offers many advantages over diffusion for the introduction of impurity atoms into semiconductor wafer and has become a workhorse technology in modern integrated-circuit fabrication. In this section, we first briefly introduce the implantation system and theories. Then source/drain and channel doping profiles are predicted by doing theoretical calculations and software simulation for the parameters that we use in the implantation. Based on the doping profile calculated, other MESFET parameters such as barrier height, built-in potential and sheet resistance are also calculated in the following sections.

2.2.1 Implantation System

An ion implanter is a high voltage particle accelerator producing a high-velocity beam of impurity ions which can penetrate the surface of semiconductor target wafer. The basic parts of the system are shown schematically in Figure 2.2. This system includes: ion source, mass spectrometer, high voltage accelerator, scanning system, target chamber.

![Schematic of ion implanter](image)
2.2.2 Mathematical model for ion implantation

As an ion enters the surface of the wafer, it collides with atoms in the lattice and interacts with electrons in the crystal. Each nuclear or electronic interaction reduces the energy of the ion until it finally comes to rest within the target. Interaction with the crystal is a statistical process, and the implanted impurity profile can be approximated by the Gaussian distribution function. The distribution is described mathematically by

\[
N(x) = N_p e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}}
\]

(2.1)

where

- \(N_p\) = peak concentration
- \(R_p\) = projected range
- \(\Delta R_p\) = projected range straggle

\(R_p\) is called the projected range and is equal to the average distance an ion travels before it stops. The peak concentration \(N_p\) occurs at \(x = R_p\). Because of the statistical nature of the process, some ions will be “lucky” and will penetrate beyond the projected range \(R_p\), and some will be “unlucky” and will not make it as far as \(R_p\). The spread of the distribution is characterized by the standard deviation \(\Delta R_p\), called the straggle.

The total number of ion implantation per unit area is the implanted dose \(Q\), which can be calculated from the integration of impurity concentration under the curve, given by

\[
Q = \sqrt{2\pi N_p \Delta R_p}
\]

(2.2)

Implantation doses can range from \(10^{10}\) /cm\(^2\) to \(10^{18}\) /cm\(^2\), and ion implantation is often used to replace the pre-deposition step in a two-step diffusion process. Doses in the range of \(10^{10}\) /cm\(^2\) to \(10^{13}\) /cm\(^2\) are required for threshold adjustment in MOS technologies and are almost impossible to achieve using diffusion.

2.2.3 Implantation calculation

The implant parameters used in our laboratory to fabricate the n-GaAs MESFET are summarized in the table 2.1.

<table>
<thead>
<tr>
<th>Ion species</th>
<th>Ion energy</th>
<th>Implant dose</th>
<th>Resist thickness</th>
<th>SiN thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel implant</td>
<td>Si(^+)</td>
<td>180 keV</td>
<td>(5 \times 10^{12}) /cm(^2)</td>
<td>1.6 µm</td>
</tr>
<tr>
<td>Source/Drain implant</td>
<td>Si(^+)</td>
<td>200 keV</td>
<td>(2 \times 10^{13}) /cm(^2)</td>
<td>0.7 µm</td>
</tr>
</tbody>
</table>

Table 2.1 Implant parameters
Because ions enter resist first and lose most energy in resist, we can simplify multi-layer situation by treating it as consisted of one outermost layer and get pretty good approximation. Then projection range \( R_p \) and projection range straggle \( \Delta R_p \) in photoresist or silicon nitride layer can be found from chart for given implant ion energy. The \( R_p \) and \( \Delta R_p \) for Si ion in photoresist, SiN and GaAs for given implant energy is shown in table 2.2.

<table>
<thead>
<tr>
<th>Energy</th>
<th>Photoresist</th>
<th>Silicon Nitride</th>
<th>Gallium Arsenide</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( R_p )</td>
<td>( \Delta R_p )</td>
<td>( R_p )</td>
</tr>
<tr>
<td>180 keV</td>
<td>0.8170</td>
<td>0.1248</td>
<td>0.1548</td>
</tr>
<tr>
<td>200 keV</td>
<td>0.9082</td>
<td>0.1339</td>
<td>0.1724</td>
</tr>
</tbody>
</table>

Table 2.2 \( R_p \) and \( \Delta R_p \) parameters for Si ion in Photo resist, SiN and GaAs (\( \mu \)m)

**a) Silicon implant profile for the channel implant (resist-masked region)**

The implant parameters from the table (Si in Photo resist) are 

\[
R_p = 0.8170 \text{ microns}
\]
\[
\Delta R_p = 0.1248 \text{ microns}
\]

Photo resist thickness \( x_r = 1.6 \text{\( \mu \)m} \)

Silicon nitride thickness \( x_n = 100 \text{ nm} \)

Peak concentration

\[
N_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} = \frac{5 \times 10^{12}}{\sqrt{2\pi} \times (0.1248 \times 10^{-4} \text{cm})} = 1.6 \times 10^{17} / \text{cm}^3
\]

Considering 35% activation,

\[
N_p = (0.35) \times 1.6 \times 10^{17} / \text{cm}^3 = 5.6 \times 10^{16} / \text{cm}^3
\]

The implantation profile will be Gaussian and is given by

\[
N(x) = N_p e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}}
\]

\[
= 5.6 \times 10^{16} / \text{cm}^3 e^{-\frac{(x-0.817\mu)^2}{2(0.1248\mu)^2}}
\]

The value of the doping concentration at the GaAs surface can be calculated from the above expression with the value of \( x = 1.6 \text{ \( \mu \)m} + 100 \text{ nm} = 1.7 \text{ \( \mu \)m} \) as follows.

\[
N(x = 1.7 \text{ \( \mu \)m}) = 5.6 \times 10^{16} / \text{cm}^3 \times \left(1.7 - 0.817\mu\right)^2 = 7.5 \times 10^5 / \text{cm}^3
\]

The doping profile is shown in the figure 2.3.
b) Silicon implant profile for the channel implant (without resist)

The implant parameters from the table (180keV, Si in SiN) are

\[ R_p = 0.1548 \text{ microns} \]
\[ \Delta R_p = 0.0432 \text{ microns} \]

Silicon nitride: 100 nm

Location of the peak concentration

\[ x_P = 0.1548 - 0.1 = 0.0548 \text{ microns} = 54.8 \text{ nm} \]

The peak concentration is given by

\[ N_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} \]
\[ = \frac{5 \times 10^{12} \text{ cm}^{-2}}{\sqrt{2\pi} (0.0432 \times 10^{-4} \text{ cm})} = 4.62 \times 10^{17} \text{ cm}^{-3} \]

Assuming 35% activation,

\[ N_{p'} = (0.35)(4.62 \times 10^{17}) / \text{cm}^3 = 1.62 \times 10^{17} / \text{cm}^3 \]

Implant Profile
The doping concentration at GaAs surface (x=0) is given by

\[
N(x) = N_B e^{\frac{-x^2}{2\Delta R_p^2}} = N_B e^{\frac{-x^2}{2\Delta R_p^2}} e^{\frac{-(x-0.0548\mu)^2}{2(0.0432\mu)^2}} = 1.62 \times 10^{17} / cm^3
\]

The doping concentration at GaAs surface (x=0) is given by

\[
N(x = 0) = 1.62 \times 10^{17} / cm^3 e^{\frac{-(0-0.0548\mu)^2}{2(0.1248\mu)^2}} = 7.2 \times 10^{16} / cm^3
\]

The junction depth \(x_j\) where \(N(x) = N_B = 1 \times 10^{14} / cm^3\) is given by

\[
N(x_j) = 1.62 \times 10^{17} / cm^3 e^{\frac{-(x_j-0.0548\mu)^2}{2(0.0432\mu)^2}} = 1.0 \times 10^{14} / cm^3
\]

\[
x_j = 0.0548\mu + (0.0432\mu) \sqrt{2 \ln \frac{1.62 \times 10^{17}}{1.0 \times 10^{14}}} = 0.221\mu
\]

The plot is shown in figure 2.4.

![Channel Implant profile through SiN](image)

**Figure 2.4** Channel Implant profile through SiN

c) Silicon implant profile for the source/drain implant (resist-masked region)

The Implant parameters for Si ion in photo resist (200 keV, Si in Photo resist) are

\[
R_p = 0.9082 \text{ microns },
\]

\[
\Delta R_p = 0.1339 \text{ microns}
\]

Photo resist thickness, \(t_1 = 0.8\mu\m
Silicon nitride thickness, \(t_2 = 100\text{ nm}\)
The location of the peak concentration is given by

\[ x_p = R_p - t_1 - t_2 = 0.9082 - 0.8 - 0.1 = 0.0082 \, \mu m = 8.2 \, nm \]

The value of the peak concentration is calculated as follows.

\[ N_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} \]

\[ = \frac{2 \times 10^{13} / cm^2}{\sqrt{2\pi} (0.1339 \times 10^{-4} cm)} = 5.96 \times 10^{17} / cm^3 \]

Assuming 35% activation,

\[ N_p = (0.35)(5.96 \times 10^{17} / cm^3) = 2.09 \times 10^{17} / cm^3 \]

The final Source / Drain Implant Profile is given by

\[ N(x) = N_p e^{\frac{-\left(x-x_p\right)^2}{2\Delta R_p^2}} = N_p e^{\frac{-\left(x-t_1-t_2-R_p\right)^2}{2\Delta R_p^2}} \]

\[ = 2.09 \times 10^{17} / cm^3 e^{\frac{-\left(x-0.0082 \mu m\right)^2}{2(0.1339 \mu m)^2}} \]

The doping concentration at the GaAs surface (x=0) is now given by

\[ N(x = 0) = 2.09 \times 10^{17} / cm^3 e^{\frac{-\left(x-0.0082 \mu m\right)^2}{2(0.1339 \mu m)^2}} = 2.086 \times 10^{17} / cm^3 \]

The Source / Drain doping plot is shown in the figure 2.5.

![Source/Drain Implant profile for resist-masked region](image_url)
d) Silicon implant profile for the source/drain implant (without resist)

For the source/drain implant with a dose of \(2 \times 10^{13} \text{ cm}^{-3}\) through the SiN, the implant parameters (200 keV, Si in SiN) are

\[
R_p = 0.1724 \text{ microns}
\]
\[
\Delta R_p = 0.0465 \text{ microns}
\]
Silicon nitride: 65 nm

Peak concentration location
\[x_p = 172.4 - 65 = 107.4 \text{ nm}\]

The peak concentration is given by
\[
N_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} = \frac{2 \times 10^{13} \text{ cm}^{-2}}{\sqrt{2\pi} \times (0.0465 \times 10^{-4} \text{ cm})} = 1.716 \times 10^{18} \text{ cm}^{-3}
\]

Assuming 35% activation
\[
N_p = (0.35)(1.716 \times 10^{18}) \text{ cm}^{-3} = 6.0 \times 10^{17} \text{ cm}^{-3}
\]

Implant Profile
\[
N(x) = N_p e^{-\frac{(x-x_p)^2}{2\Delta R_p^2}} = N_p e^{-\frac{(x-x_p)^2}{2\Delta R_p^2}}
\]
\[
= 6.0 \times 10^{17} \text{ cm}^{-3} e^{-\frac{(x-x_p)^2}{2\Delta R_p^2}}
\]

Considering the channel implant, the total silicon concentration profile
\[
N(x) = 6.0 \times 10^{17} \text{ cm}^{-3} e^{-\frac{(x-x_p)^2}{2\Delta R_p^2}} + 1.62 \times 10^{17} \text{ cm}^{-3} e^{-\frac{(x-x_p)^2}{2\Delta R_p^2}}
\]

The plot is shown in figure 2.6. We can read the total peak concentration from the figure
\[
N_{\text{peak}} = 6.863 \times 10^{17} \text{ cm}^{-3}
\]

Determination of total concentration at GaAs surface \((x=0)\)
\[
N(x=0) = 6.0 \times 10^{17} \text{ cm}^{-3} e^{-\frac{(0-x_p)^2}{2\Delta R_p^2}} + 7.2 \times 10^{16} \text{ cm}^{-3} = 1.14 \times 10^{17} \text{ cm}^{-3}
\]

Determination of junction depth \(x_j\) where \(N(x) = N_B\). For \(N_B = 1 \times 10^{14} \text{ cm}^{-3}\), the figure in log scale is shown in figure 2.7, and we can read the junction depth from the figure as
\[x_j = 0.3 \mu\]

Comparing these results with those for the channel implant, we can see the peak concentration and junction depth of source/drain implant is bigger because of higher dose and implant energy.
Figure 2.6  Total implant profile in the Source / Drain Region

Figure 2.7  Determination of junction depth in the S/D regions
2.3 Sheet resistance

Sheet resistance for channel implant region:

From the channel implant calculation in the last section, we have

- Implant energy, $E_i = 180$ kev
- Peak concentration, $N_p = 1.62 \times 10^{17} /\text{cm}^3$
- Surface concentration, $N_s = 7.2 \times 10^{16} /\text{cm}^3$
- Junction depth, $X_j = 0.221 \ \mu\text{m}$
- Silicon nitride thickness, $X_{SiN} = 0.1 \ \mu\text{m}$

Now, from the given relation, we have

$$X / X_j = X_{SiN} / (X_j + X_{SiN}) = 0.1 / (0.221 + 0.1) \approx 0.31 \approx 0.3$$

Using the value of $X/X_j$ and $N_s$, we can read the value of average conductivity $\bar{\sigma}$ directly from the plot of $N_s$ vs $\bar{\sigma}$ (figure 2.8) for different values of $X/X_j$, we have

$\bar{\sigma} = 12 / (\Omega\cdot\text{cm})$

Now, from the given relation, the sheet resistance is given by

$$R_s = \frac{1}{\bar{\sigma}X_j} = \frac{1}{12 / (\Omega\cdot\text{cm}) \times 0.221 \times 10^{-4} \text{cm}} = 3.8 \times 10^3 \Omega / \text{square}$$

Sheet resistance for source/drain implant region:

For the Source / Drain region we have,

- $E_i = 200$ keV, and
- $N_p = 6.86 \times 10^{17} /\text{cm}^3$
- $N_s = 1.14 \times 10^{17} /\text{cm}^3$
- $X_j = 0.3 \ \mu\text{m}$
- $X_{SiN} = 0.065 \ \mu\text{m}$

$$X / X_j = X_{SiN} / (X_j + X_{SiN}) = 0.065 / (0.3 + 0.065) \approx 0.178 \approx 0.2$$

Using the value of $X/X_j$ and $N_s$, we can read the value of average conductivity, $\bar{\sigma}$ using the plot of $N_s$ vs $\bar{\sigma}$ for different values of $X/X_j$ as shown in the figure 2.7, we have

$\bar{\sigma} = 22 / (\Omega\cdot\text{cm})$

Now, from the given relation, the sheet resistance is given by

$$R_s = \frac{1}{\bar{\sigma}X_j} = \frac{1}{2.2 \times 10^4 \times 0.3 \times 10^{-4}} = 1.5 \times 10^3 \Omega / \text{square}$$

The figure 2.8 shows the plot of the data to read $\bar{\sigma}$ (inner blue lines for channel implant and red for S/D).
Figure 2.8 Surface concentration vs. average conductivity for different X/Xj. The two lines show the values read for average conductivity

2.4 Gate built-in potential, Pinchoff and Threshold voltage

The gate – channel built-in potential is given by

\[ V_{bi} = \Phi_m - \left[ \chi + \frac{E_g}{2q} - \frac{k_BT}{q} \ln \left( \frac{N_D}{n_i} \right) \right] \]  \hspace{1cm} (2.3)

where

- \( \Phi_m \) = Gate metal (Al) work function = 4.4 V
- \( \chi \) = Electron Affinity of GaAs = 4.04 V
- \( E_g \) = Energy bandgap of GaAs = 1.42 eV
- \( n_i \) = Intrinsic carrier concentration of GaAs = 8.7x10^5/cm^3
- \( N_D \) = channel doping (use \( N_s = 7.2 \times 10^{16} /\text{cm}^3 \))
- \( q = 1.6x10^{-19} \text{ C} \)
- \( k_B = 1.38x10^{-23} \text{ J/K} \)
- \( T = 300^\circ\text{K} \)

Also, substituting these values in the expression for \( V_{bi} \), we get

\( V_{bi} = 0.3 \text{ V.} \)
Using the values for peak channel doping and implant energy as follows

\begin{align*}
\text{Implant energy, } & \quad E_i = 180 \text{ keV} \\
\text{Peak concentration, } & \quad N_p = 1.62 \times 10^{17} /\text{cm}^3
\end{align*}

We can read the value for pinchoff voltage from the figure 2.9

\[ V_p \approx 2.5 \text{ V}. \]

The figure 2.8 shows the method of calculating the pincoff voltage.

Now, the threshold voltage is given by

\[ V_T = V_{bi} - V_p = 0.13024 - 2.5 = -2.2 \text{ V} \]

2.5 Conclusion

Some simulation results from Silvaco’s Athena fab. simulator for the Channel and Source/Drain implant profiles using the same parameters as those used in the theoretical calculations above are presented here for the comparison purposes.

For channel implant through SiN (Si in GaAs) we have

\begin{align*}
E_i & = 180 \text{ keV} \\
Q & = 5 \times 10^{12} /\text{cm}^2 \\
\text{SiN cap layer} & = 100 \text{ nm} \\
35 \% \text{ activation}
\end{align*}

Simulation results:

\[ N_p = 6.15 \times 10^{16} /\text{cm}^3 \]
Peak location = 0.26 – 0.1 = 0.16 µm

Surface concentration in GaAs,
\[ N(x=0) = 3.5 \times 10^{16} /\text{cm}^3 \]
Junction depth (\( N_B = 10^{15} /\text{cm}^3 \)) in GaAs,
\[ X_j = 0.6 - 0.1 = 0.5 \text{ µm} \]

The simulation plot is shown in the figure 2.10.

![Simulation plot](image)

Figure 2.9 Silvaco’s Athena fab simulation result for Channel implant

For source / Drain implant (Si in GaAs), the parameters are
- \( E_i = 200 \text{ keV} \)
- \( Q = 2 \times 10^{13} /\text{cm}^2 \)
- SiN cap layer = 65 nm
- 35% activation

Simulation results:
\[ N_P = 1.14 \times 10^{17} /\text{cm}^3 \]
Peak location = 0.284 – 0.065 = 0.219 µm

Surface concentration in GaAs,
\[ N(x=0) = 1.06 \times 10^{16} /\text{cm}^3 \]
Junction depth (\( N_B = 10^{15} /\text{cm}^3 \)) in GaAs,
\[ X_j = 0.68 - 0.065 = 0.615 \text{ µm} \]
The simulation plot is shown in the figure 2.11.

Figure 2.11  Silvaco’s Athena fab simulation result for S/D implantation

As seen above, the simulation results are in agreement with those calculated. Some values such as junction depth are not consistent which is due to the use of different masking materials and the different thickness. So our theoretical calculations are consistent to those values obtained from the Silvaco’s Athena fab simulator.
Chapter 3  Fabrication Results and Test Structure Measurements

3.1  Introduction

This chapter describes in brief the fabrication process summary. The exact equipment settings for each process are given. The results of different tests and the sample calculations are also shown given in this chapter. The problems encountered during the experiment and the possible solutions are also described here when ever possible. The chapter will conclude with comparisons of experimental results with the theoretical calculations.

3.2  Fabrication Process Summary

As discussed in chapter 2, this schedule describes a four-mask, double implant process for formation of n-GaAs MESFETs with implanted channels. The four mask levels are:
1. Channel implant,
2. Source / drain implant,
3. Ohmic contact formation and
4. Schottky gate formation.

The masks are all light field and positive resist is used throughout the process.

1. Initial wafer cleaning (SOP # 200).
2. Silicon nitride cap deposition by reactive sputtering (SOP # 210).
   Cap thickness = 100 nm
3. Pre-bake: 120°C for 15 minutes
4. Resist patterning using positive resist (SOP # 120, 122, 123, 124B, 126 and 127)
   Adhesion promoter (HMDS): P20

<table>
<thead>
<tr>
<th>Process</th>
<th>Photo resist</th>
<th>5 sec. Spread Cycle (rpm)</th>
<th>30 sec. Spin Cycle (rpm)</th>
<th>Target thickness (μm)</th>
</tr>
</thead>
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<tr>
<td>Channel Implant</td>
<td>S1818</td>
<td>500</td>
<td>5000</td>
<td>1.6</td>
</tr>
<tr>
<td>Source / Drain Implant</td>
<td>S1807</td>
<td>500</td>
<td>4000</td>
<td>0.7</td>
</tr>
<tr>
<td>Ohmic contact formation</td>
<td>S1807</td>
<td>500</td>
<td>4000</td>
<td>0.7</td>
</tr>
<tr>
<td>Schottky gate formation</td>
<td>S1818</td>
<td>500</td>
<td>5000</td>
<td>1.6</td>
</tr>
</tbody>
</table>
5. Soft bake (SOP # 123):
   Temperature: 95°C
   Time: 30 minutes

6. Mask alignment and exposure (SOP # 124):
   Aligner: Suss MJB-3 Optical Mask Aligner
   Wavelength of UV light: 405 nm
   Exposure type: Contact printing

<table>
<thead>
<tr>
<th>Mask #</th>
<th>Exposure time (sec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Channel Implant</td>
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</tr>
<tr>
<td>2. Source / Drain Implant</td>
<td>6</td>
</tr>
<tr>
<td>3. Source / Drain metallization</td>
<td>6</td>
</tr>
<tr>
<td>4. Gate metallization</td>
<td>12</td>
</tr>
</tbody>
</table>

   Three modes of exposure:
   1. Contact Printing: Wafer directly in contact with the mask
   2. Proximity Printing: 20 – 50 micron separation between wafer and mask
   3. Projection Printing: Wafer separated from mask by lens

7. Chlorobenzene treatment for metal liftoff for 90 seconds and blow-dry with N₂ gas.

8. Photo resist pattern development (SOP # 125B):
   Developer: Shipley 351
   Development time: 1 minute in Sp351 and rinse 1 minute in DI water
   Blow-dry with N₂ gas

9. Hard bake (SOP # 127):
   Temperature: 95°C
   Time: 15 minutes

9. Silicon ion implantation (SOP # 202)

<table>
<thead>
<tr>
<th>Process</th>
<th>Implant Energy (KeV)</th>
<th>Dose (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Implant</td>
<td>180</td>
<td>5x10¹²</td>
</tr>
<tr>
<td>Source / Drain Implant</td>
<td>200</td>
<td>2x10¹⁴</td>
</tr>
</tbody>
</table>

10. Shallow etching of silicon nitride (≈ 50nm) for alignment registration purposes in buffered HF solution and plasma etching (SOP # 210):
    Plasma etching parameters:
    Gas: 9.6 sccm of CF4 + 0.4 sccm of O2
    RF power: 100W
    Frequency: 30 KHz
    Time: 30 seconds
11. Resist stripping and ashing in oxygen plasma:
    Resist stripping:
    5 minutes in 40°C hot Acetone
    1 minute in DI water
    Blow-dry with N₂ gas
    Plasma ashing with 20 sccm O₂, 100W, 30KHz for 5 minutes

10. Annealing of ion implants using rapid thermal annealing (SOP # 203).
    Maximum temperature = 850 °C
    Ambient = forming gas
    Time = 120 seconds

11. Silicon nitride etching for Ohmic contacts.
    1. CF₄ plasma etching to semiconductor surface.
        a. Gas: 9.6 sccm CF₄ + 0.4 sccm O₂
        b. Power and time: 150 W for 2 minutes and 100 W for 1 minute
    2. Final wet etch cleaning of exposed GaAs surface in 50 %HCl for 1 minute (SOP # 210).

12. Deposition of AuGe/Ni metal for Ohmic contacts to source and drain using E-beam evaporation and patterning by liftoff technique (SOP # 207 & 208).

13. Ohmic contact alloying by rapid thermal heating (SOP # 203).
    Maximum temperature = 480 °C
    Ambient = forming gas
    Time = 120 seconds

    1. CF₄ plasma etching to semiconductor surface.
    2. Final wet etch cleaning of exposed GaAs surface in 50 %HCl (SOP # 210).

15. Aluminum metal deposition for Schottky gate formation using e-beam evaporation and patterning by liftoff technique (SOP # 207 & 208).

The basic fabrication process for constructing GaAs MESFETs uses a simple four-mask, double ion implantation process as shown in Figure 3.1.

The main process summaries can be explained using the following set of figures. The figure 3.1 gives the over view of the whole fabrication process. This figure summarizes the process starting from the initial GaAs wafer and the ending with the final device. The
channel implant process is described in detail by the figure 3.2. This figure also shows the cross-section of the wafer at each step. The processes starting from the resist application to the Silicon Nitride etching are described in this figure. The Source / Drain implant processes are summarized in the figure 3.3. This figure also shows the detail cross-section and the top view of the wafer at each step of the process.

An important process of the MESFET fabrication process is the Mask and wafer alignment and the exposure. A special technique used to make sure of the alignment of all of the dies on the wafer is the Split-Field alignment. This technique allows us to view two different sites at a time and align them. This technique is shown in the figure 3.5. This figure also shows the Optical Mask Aligner in our laboratory.

Figure 3.1 Summary of the MESFET Fabrication Process
Figure 3.2  Channel Implant Process
Figure 3.3   Source – Drain Implant Process
3.3 Sheet Resistance Measurement

In order to evaluate the device variation due to the effects resulting from the design or process phases, it is necessary to make sheet resistance measurements using the Van Der Pauw structures (device #1 for Channel region device #2 for Source/Drain region) fabricated on the wafer. The quality of the MESFET depends heavily on the quality of the contacts. Using the four-point method, the sheet resistance of the implanted layer can be calculated using the expression given below:

\[
R_s = \frac{\prod V_4 - V_3}{\ln(2) I_{12}}
\]  

(3.1)

Where \(I_{12}\) is the current forced through the probe 1 and 2 and \(V_4\) and the \(V_3\) are the voltage sensed between probes 3 and 4.
Table 3.1  Data for I – V curve for Source/Drain Van Der Pauw

<table>
<thead>
<tr>
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<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>-100</td>
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<tr>
<td>100</td>
<td>0.0189</td>
<td>100</td>
<td>0.0193</td>
</tr>
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</table>
Figure 3.5 Plot for I-V curve for Source/Drain Van Der Pauw

The data for the current - voltage characteristics for the Source / Drain are listed in the table 3.1 and the plots are shown in Figure 3.1.

Similarly the data and the plots for the current – voltage characteristics for the channel Van Der Pauw are shown in the table 3.2 and figure 3.2 respectively.
Table 3.2 I – V data for Channel Van Der Pauw.

<table>
<thead>
<tr>
<th></th>
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<td>0.043</td>
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<tr>
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<tr>
<td>10</td>
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<td>10</td>
<td>0.115</td>
<td>1.5</td>
<td>0.003</td>
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<td>0.25</td>
<td>12</td>
<td>0.23</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.6 I – V plots for Channel Van Der Pauw.
The I–V plots for both of the Source / Drain and the Channel Van Der Pauw are clearly showing a linear nature. This shows that the contact for the Source / Drain Van Der Pauw are Ohmic-like whereas those for channel Van Der Pauw are slightly different. The standard deviations for both Van Der Pauws are also shown on the tables. The resistances calculated from the I-V curves are shown in the table 3.3 and table 3.4 for Source / Drain and Channel Van Der Pauw respectively.

<table>
<thead>
<tr>
<th>dI/dV (μA/mV)</th>
<th>σ</th>
<th>R (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I: AA-Y; V: U-W</td>
<td>5.29883</td>
<td>0.27415</td>
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<tr>
<td>I: W-Y; V: AA-U</td>
<td>5.19376</td>
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<tr>
<td>I: U-W; V: AA-Y</td>
<td>5.27837</td>
<td>0.21074</td>
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</tbody>
</table>

Table 3.3 Resistance calculation for source-drain Van Der Pauw from I-V curve

<table>
<thead>
<tr>
<th>dI/dV (μA/mV)</th>
<th>σ</th>
<th>R (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I: U-W; V: AA-Y</td>
<td>0.29178</td>
<td>2.52054</td>
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<tr>
<td>I: AA-U; V: W-Y</td>
<td>0.568</td>
<td>1.46061</td>
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<tr>
<td>I: AA-Y; V: U-W</td>
<td>0.48066</td>
<td>0.85148</td>
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</tbody>
</table>

Table 3.4 Resistance calculation for channel Van Der Pauw from I-V curve

<table>
<thead>
<tr>
<th>Site #</th>
<th>Input I(μA)</th>
<th>Out: AA-U</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>Out: AA-Y</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>Out: W-Y</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>Out: W-U</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>( \bar{R}_s(Ω) )</th>
<th>σ_{R_s}(Ω)</th>
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<td>132</td>
<td>598.2</td>
<td>594.8</td>
<td>4.3</td>
<td>4.3</td>
<td>4.3</td>
<td>4.3</td>
<td>4.3</td>
</tr>
<tr>
<td>5</td>
<td>0.1</td>
<td>8</td>
<td>362.6</td>
<td>13</td>
<td>589.2</td>
<td>11</td>
<td>498.5</td>
<td>10</td>
<td>453.2</td>
<td>475.9</td>
<td>94.3</td>
<td>94.3</td>
<td>94.3</td>
<td>94.3</td>
<td>94.3</td>
</tr>
</tbody>
</table>

Table 3.5 Sheet resistance calculation for five different sites of Source/Drain Van Der Pauw structure

The sheet resistances calculated for the two Van Der Pauw are shown on the table 3.5 and table 3.6. Clearly the Source / Drain Van Der Pauw has low sheet resistance which is
in the order of few hundreds where as those calculated for the Channel Van Der Pauw are in the order of few thousands.

<table>
<thead>
<tr>
<th>Site #</th>
<th>Input I(μA)</th>
<th>In: W-Y</th>
<th>Out: AA-U</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>In: W-U</th>
<th>Out: AA-Y</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>In: AA-U</th>
<th>Out: W-Y</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>In: AA-Y</th>
<th>Out: W-U</th>
<th>V (μV)</th>
<th>R_s (Ω)</th>
<th>( \bar{R_s} (\Omega) )</th>
<th>( \sigma_{R_s} (\Omega) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>25.45</td>
<td>1.15E+01</td>
<td>25.85</td>
<td>1.17E+01</td>
<td>27.03</td>
<td>1.23E+01</td>
<td>26.7</td>
<td>1.21E+01</td>
<td>1.19E+04</td>
<td>3.32E+02</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>7.81</td>
<td>3.54E+01</td>
<td>6.97</td>
<td>3.16E+01</td>
<td>8.83</td>
<td>4.00E+01</td>
<td>9.72</td>
<td>4.41E+01</td>
<td>3.78E+04</td>
<td>5.43E+03</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1.13</td>
<td>5.12E+06</td>
<td>1.3</td>
<td>5.89E+06</td>
<td>2.19</td>
<td>9.93E+06</td>
<td>2.1</td>
<td>9.52E+06</td>
<td>7.61E+03</td>
<td>2.46E+03</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>131.4</td>
<td>5.96E+08</td>
<td>101.7</td>
<td>4.61E+08</td>
<td>115.3</td>
<td>5.23E+08</td>
<td>129.5</td>
<td>5.87E+08</td>
<td>5.41E+05</td>
<td>6.28E+04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>19.36</td>
<td>8.77E+07</td>
<td>18.46</td>
<td>8.37E+07</td>
<td>24.38</td>
<td>1.10E+08</td>
<td>29.7</td>
<td>1.35E+08</td>
<td>1.04E+05</td>
<td>2.35E+04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.6  Sheet resistance calculations for five different sites of Channel Van Der Pauw structure

3.4 TLM Measurement of Sheet Resistance

The TLM measurements data at five test sites with the calculated resistances are shown in the table 3.7. The average values for the resistance at five different sites are shown in the table 3.8. From dimensions measurements, we get the exact length of the spacing d (also shown in table 3.8).

Width of the contact region W = 0.0020 inch = 0.00508 cm,
Width of the metal contacts L = 0.0006~0.0007 inch = 0.001524 ~ 0.001778 cm

The plot for the average resistance at each contact spacing versus the contact spacing is shown in the figure 3.3. The slope and standard deviation is marked in the plot. We can see that we have smaller deviation for the case not considering L.

So we can calculate the sheet resistance (not considering L)

\[
R_s = \frac{R \times W}{d} = \frac{\Delta R}{\Delta d} \times W = 383.58854 \times 0.0020 = 0.767k\Omega \quad \text{square} = 767\Omega \quad \text{square}
\]

It is consistent with the Van Der Pauw measurements,

\[
R_s = 800 \pm 200\Omega
\]
<table>
<thead>
<tr>
<th>Site #</th>
<th>Spacing</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
<th>Resistance (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>1X</td>
<td>0.1</td>
<td>0.14970</td>
<td>0.6680</td>
</tr>
<tr>
<td></td>
<td>2X</td>
<td>0.1</td>
<td>0.07987</td>
<td>1.2520</td>
</tr>
<tr>
<td></td>
<td>3X</td>
<td>0.1</td>
<td>0.05268</td>
<td>1.8983</td>
</tr>
<tr>
<td></td>
<td>4X</td>
<td>0.1</td>
<td>0.03470</td>
<td>2.8818</td>
</tr>
<tr>
<td></td>
<td>5X</td>
<td>0.1</td>
<td>0.02848</td>
<td>3.5112</td>
</tr>
<tr>
<td></td>
<td>7X</td>
<td>0.1</td>
<td>0.02109</td>
<td>4.7416</td>
</tr>
<tr>
<td>#2</td>
<td>1X</td>
<td>0.1</td>
<td>0.17915</td>
<td>0.5582</td>
</tr>
<tr>
<td></td>
<td>2X</td>
<td>0.1</td>
<td>0.09000</td>
<td>1.1111</td>
</tr>
<tr>
<td></td>
<td>3X</td>
<td>0.1</td>
<td>0.06070</td>
<td>1.6474</td>
</tr>
<tr>
<td></td>
<td>4X</td>
<td>0.1</td>
<td>0.04630</td>
<td>2.1598</td>
</tr>
<tr>
<td></td>
<td>5X</td>
<td>0.1</td>
<td>0.03730</td>
<td>2.6810</td>
</tr>
<tr>
<td></td>
<td>7X</td>
<td>0.1</td>
<td>0.02650</td>
<td>3.7736</td>
</tr>
<tr>
<td>#3</td>
<td>1X</td>
<td>0.1</td>
<td>0.11670</td>
<td>0.8569</td>
</tr>
<tr>
<td></td>
<td>2X</td>
<td>0.1</td>
<td>0.05690</td>
<td>1.7575</td>
</tr>
<tr>
<td></td>
<td>3X</td>
<td>0.1</td>
<td>0.03862</td>
<td>2.5893</td>
</tr>
<tr>
<td></td>
<td>4X</td>
<td>0.1</td>
<td>0.03070</td>
<td>3.2573</td>
</tr>
<tr>
<td></td>
<td>5X</td>
<td>0.1</td>
<td>0.02450</td>
<td>4.0816</td>
</tr>
<tr>
<td></td>
<td>7X</td>
<td>0.1</td>
<td>0.01700</td>
<td>5.8824</td>
</tr>
<tr>
<td>#4</td>
<td>1X</td>
<td>0.1</td>
<td>0.12470</td>
<td>0.8019</td>
</tr>
<tr>
<td></td>
<td>2X</td>
<td>0.1</td>
<td>0.06540</td>
<td>1.5291</td>
</tr>
<tr>
<td></td>
<td>3X</td>
<td>0.1</td>
<td>0.04347</td>
<td>2.3004</td>
</tr>
<tr>
<td></td>
<td>4X</td>
<td>0.1</td>
<td>0.02878</td>
<td>3.4746</td>
</tr>
<tr>
<td></td>
<td>5X</td>
<td>0.1</td>
<td>0.02356</td>
<td>4.2445</td>
</tr>
<tr>
<td></td>
<td>7X</td>
<td>0.1</td>
<td>0.01747</td>
<td>5.7241</td>
</tr>
<tr>
<td>#5</td>
<td>1X</td>
<td>0.1</td>
<td>0.14320</td>
<td>0.6983</td>
</tr>
<tr>
<td></td>
<td>2X</td>
<td>0.1</td>
<td>0.06993</td>
<td>1.4300</td>
</tr>
<tr>
<td></td>
<td>3X</td>
<td>0.1</td>
<td>0.04758</td>
<td>2.1017</td>
</tr>
<tr>
<td></td>
<td>4X</td>
<td>0.1</td>
<td>0.03724</td>
<td>2.6853</td>
</tr>
<tr>
<td></td>
<td>5X</td>
<td>0.1</td>
<td>0.02991</td>
<td>3.3434</td>
</tr>
<tr>
<td></td>
<td>7X</td>
<td>0.1</td>
<td>0.02105</td>
<td>4.7506</td>
</tr>
</tbody>
</table>

Table 3.7 TLM measurements

<table>
<thead>
<tr>
<th>Spacing d (inch) (consider L)</th>
<th>Spacing d (inch) (not consider L)</th>
<th>Resistance (kΩ)</th>
<th>σ of resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1X 0.0017</td>
<td>0.0017</td>
<td>0.7167</td>
<td>0.3101</td>
</tr>
<tr>
<td>2X 0.0037</td>
<td>0.0037</td>
<td>1.4159</td>
<td>0.6183</td>
</tr>
<tr>
<td>3X 0.006</td>
<td>0.0054</td>
<td>2.1074</td>
<td>0.9170</td>
</tr>
<tr>
<td>4X 0.0076</td>
<td>0.0076</td>
<td>2.8918</td>
<td>1.2636</td>
</tr>
<tr>
<td>5X 0.01</td>
<td>0.0093</td>
<td>3.5723</td>
<td>1.5580</td>
</tr>
<tr>
<td>7X 0.0143</td>
<td>0.013</td>
<td>4.9744</td>
<td>2.1650</td>
</tr>
</tbody>
</table>

Table 3.8 Average resistance at five sites

40
Considering width of the metal contacts L
Slope=339.91478, \( \sigma = 9.01777 \)
Intercept=0.16003, \( \sigma = 0.07498 \)

Figure 3.7  \( R_T \) vs. \( d \) plot for calculating \( R_C \)

From the equation
\[
R_T = 2R_C + R_s \frac{d}{W}
\]
the Y-intercept of the plot gives the value for \( 2R_C \). Thus for the figure
\( 2R_C = 160 \) ohms
So, \( R_C = 80 \) ohms.
3.5 Current voltage characteristic of Diodes measurement

A lot of information comes from the I-V measurements of the diode structures fabricated on the wafer. From the I-V measurement we can verify the device’s behavior in the forward and reverse bias conditions. The reverse breakdown voltage, reverse saturation current, the barrier height and the ideality factor n and be calculated from this measurement.

For diode #4 and #18, the results of I-V measurements are shown in figure 3.8 and figure 3.9. From these figures we can directly determine the reverse saturation currents as given below.

For #4: $I = 3.8 \times 10^{-6}$ A,

and for #18: $I = 5.6 \times 10^{-7}$ A.

From these curves we can verify that the Schottky diodes #4, #18 show very good diode like behavior. All the sites show the similar results and it is a good identification that the quality of diodes is uniform and good repeatability. This can tell the parameter of the channel making and Al deposition is good.
3.5.1 Breakdown of #4 and #18

From the measurement at different sites of the wafer, the breakdown characteristics of the devices are predicted. From the result, which is shown in the figure 3.10, the breakdown voltage is around 28 V and is the same for other devices.
3.5.2 Log J vs. V:

The current-voltage characteristics for Schottky diode is given by the familiar diode expression as follows,

\[ J = J_s \left( \frac{qV}{nkT} - 1 \right) \]

(3.2)

Where

\[ J_s = A T^2 e^{-\frac{\phi_B}{kT}} \]

We get the current density \( J \) by the following relationship,

\[ J = \frac{I}{A} \]

Where \( A \) is the Schottky contact area. From the optical measurements, we get the areas of Schottky contact as follows.

For device #4 \( A = 4.82 \times 10^{-4} \text{cm}^2 \),
and for device #18 \( A = 4.65 \times 10^{-4} \text{cm}^2 \).

The optical measurements for device #4 and #18 are shown in figure 3.11.
Figure 3.12  Log (J) vs. V for device #4

From the slope of the curves above we can calculate the ideality factor $n$ as follows.

$$n = \frac{q}{k_B T} \frac{\partial V}{\partial (\ln J)}$$  \hspace{1cm} (3.3)

$$n = \frac{q}{k_B T} \frac{\partial V}{\partial (\ln J)} = \frac{1}{\text{slope} \times (0.0259)}$$

### Device #4

<table>
<thead>
<tr>
<th></th>
<th>site 1</th>
<th>site 2</th>
<th>site 3</th>
<th>site 4</th>
<th>site 5</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\partial (\ln J)}{\partial V}$</td>
<td>1.34391</td>
<td>3.23921</td>
<td>1.38161</td>
<td>2.84298</td>
<td>2.73942</td>
<td>2.3 ± 0.9</td>
</tr>
</tbody>
</table>

### Device #18

<table>
<thead>
<tr>
<th></th>
<th>site 1</th>
<th>site 2</th>
<th>site 3</th>
<th>site 4</th>
<th>site 5</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\partial (\ln J)}{\partial V}$</td>
<td>3.77354</td>
<td>1.3343</td>
<td>0.57811</td>
<td>3.27287</td>
<td>3.19152</td>
<td>2.4 ±1.4</td>
</tr>
<tr>
<td>$n$</td>
<td>10.23178</td>
<td>28.93655</td>
<td>66.78666</td>
<td>11.797</td>
<td>12.0977</td>
<td>15.88846</td>
</tr>
</tbody>
</table>
Table 3.9  Ideality factor calculation

Js can be obtained from y-intercept of the Log (J)-V plots,

<table>
<thead>
<tr>
<th>Device #4</th>
<th>site 1</th>
<th>site 2</th>
<th>site 3</th>
<th>site 4</th>
<th>site 5</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Js (A/cm²)</td>
<td>0.001351</td>
<td>1.17E-07</td>
<td>0.001541</td>
<td>7.31E-07</td>
<td>1.24E-06</td>
<td>1.17E-05</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device #18</th>
<th>site 1</th>
<th>site 2</th>
<th>site 3</th>
<th>site 4</th>
<th>site 5</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Js (A/cm²)</td>
<td>1.29E-09</td>
<td>0.000215</td>
<td>0.050029</td>
<td>6.29E-09</td>
<td>3.68E-08</td>
<td>1.26E-06</td>
</tr>
</tbody>
</table>

Table 3.10  Calculations of Js

We can determine barrier height $\phi_b$ from intercept Js

$$\phi_b = \frac{k_B T}{q} \ln \left( \frac{A^{**} T^2}{J_s} \right)$$  \hspace{1cm} (3.4)

For Device #4

$$\phi_b = \frac{k_B T}{q} \ln \left( \frac{A^{**} T^2}{J_s} \right) = 0.0259 \times \ln \left( \frac{8.16 \times 300^2}{1.17 \times 10^{65}} \right) = 0.644V$$

For Device #18

$$\phi_b = \frac{k_B T}{q} \ln \left( \frac{A^{**} T^2}{J_s} \right) = 0.0259 \times \ln \left( \frac{8.16 \times 300^2}{1.26 \times 10^{65}} \right) = 0.702V$$

For GaAs,

$$N_C = 4.7 \times 10^{17} (cm^{-3})$$

$$N_D = \frac{Q}{x_j} = 5 \times 10^{12} / (0.221056 \times 10^{-4}) = 2.262 \times 10^{17} (cm^{-3})$$

$$V_n = \frac{k_B T}{q} \ln \frac{N_C}{N_D} = 0.019V$$
Then we can calculate built-in potential $V_{bi}$ for device #4 and #18 as follows.

For Device #4

$$V_{bi} = \phi_B - V_a = 0.625V$$

For Device #18

$$V_{bi} = \phi_B - V_a = 0.683V$$

These results are very close to the theoretic value for $V_{bi}$, which is 0.3V.

3.6 Capacitance-Voltage Measurement

From the Capacitance-Voltage measurement, the built-in potential $V_{bi}$ and channel doping carrier concentration $N_D$ can be obtained. The plots of C-V measurement for #20 are shown in Figure 3.13. The expression for the space charge capacitance is given by

$$C_{SC} = \varepsilon_s \frac{q \varepsilon_s N_D}{W} \left[ \frac{1}{2(V_{bi} - V)} \right]$$

From this equation we can get

$$\frac{1}{C_{SC}^2(V)} = \frac{2(V_{bi} - V)}{q \varepsilon_s N_D A^2}$$

(3.5)

![Figure 3.13 C vs. V Curve](image)

Where,

- $A$ is the capacitor area or the Schottky contact area, for #19 capacitance,
  
  $A = 4.9 \times 10^4 \ cm^2$

- $\varepsilon_s = \varepsilon_0 \varepsilon_r = (8.85 \times 10^{-14} \ Farad/\ cm) \times 13.1 = 1.16 \times 10^{-12} \ Farad/\ cm$
The calculation and plot of $\frac{1}{C_{SC}^2}$ versus the reverse bias is shown in figure 3.14.

**Figure 3.14 $\frac{1}{C_{SC}^2}$ versus the reverse bias**

**Figure 3.15 Linear fit of $1/C_{SC}^2$-V plot**
An extrapolation of the linear line is performed to get the voltage intercept and the built-in potential.

\[ V_{bi} = 1.37 \text{ V} \]

\[ \phi_{m} = \phi_{d} - \chi = V_{bi} + \phi_{s} - \chi = V_{bi} + \frac{E_{g}}{2q} - \frac{k_{B}T}{q} \ln \left( \frac{N_{D}}{n_{i}} \right) \]

\[ = V_{bi} + \frac{1.42}{2} V - (0.0259V) \ln \left( \frac{7.2E16}{8.7E5} \right) = V_{bi} + 0.06V \]

So the barrier height is 1.43V

The Channel Doping Profile \( (N_{D} \text{ vs. } W) \) can now be obtained from the following expressions. The plot for the resulting channel doping is shown in the figure 3.15.

\[
N_{D}(W) = \frac{2}{q\varepsilon_{s} A^{2}} \left\{ \frac{-1}{\frac{d(1/C_{sc}^{2})}{dV}} \right\} \quad (3.6)
\]

\[
W(V) = \frac{\varepsilon_{s} A}{C_{sc}(V)} \quad (3.7)
\]
Figure 3.15  Channel Doping profile obtained from C-V plot

3.7 Conclusion

Most of the measurements and calculations shown in this chapter are consistent with the theoretical values. The experimentally measured values shown in this chapter show, in general close agreement with those calculated theoretically in the previous chapter. There are few exceptions where we had to do minor adjustments to get the consistent results. For example the channel C – V data from the first time measurement was completely unexpected. This might be due to improper channel doping. To obtain above-mentioned results we took the readings in a fresh wafer. The fabrication of the device in the lab was successful.

One thing we clearly see that the channel implantation might have some problem. This is because the measurement data for channel sheet resistance and also the C-V data are not consistent to the theoretical expectation. But the Source / Drain implantation seems to be pretty good. This can be verified from the sheet resistance measurement data given above.
Chapter 4 MESFET measurements

4.1 MESFET Current-Voltage Characteristics

4.1.1 Introduction

The typical $I-V$ characteristics of an n-channel depletion mode (normally on) MESFET are shown in Figure 4.1. Drain current flows for gate-source voltages $V_{GS}$ that are less negative than a threshold voltage $V_T$. For a given channel of uniform doping $N_D$ and dielectric permittivity $\varepsilon_s$, the Schottky-barrier depletion equation may be used to define a pinch-off voltage $V_{Po}$, given by

$$V_{Po} = \frac{qN_Dh^2}{2\varepsilon_s}$$

which represents the net potential required to deplete a channel of thickness $h$ under the gate. The threshold voltage is then defined as

$$V_T = V_{bi} - V_{Po}$$

where $V_{bi}$ is the Schottky-barrier built-in voltage, given by

$$V_{bi} = \phi_m - \phi_s = \phi_m - \left[\phi_m + \frac{E_g}{2q} - \frac{k_B T}{q} \ln \left( \frac{N_D}{n_i} \right) \right]$$

where $\phi_m$ is the Gate metal (Al) work function (4.4 V), $\chi$ is Electron Affinity of GaAs (4.04 V) and $E_g, n_i$ are Energy bandgap and Intrinsic carrier concentration (1.42 eV, 8.7x10^5/cm^3 for GaAs).
The dashed parabola in Figure 4.1 is the locus of saturation voltage. The saturation voltage $V_{Dsat}$ is the drain-source voltage at which the drain current saturates for a given $V_{GS}$, given by

$$V_{Dsat} = V_{Po} - V_{bi} + V_{GS}$$  \hspace{1cm} (4.4)

The region to the left of this parabola is known as the linear region because, for a given gate voltage, the drain current is linear with $V_{DS}$ until saturation effects become dominant as $V_{Dsat}$ is approached. The region between the parabola and avalanche breakdown is known as the saturation region.

We can calculate the $I_D (V_{GS}, V_{DS})$ equations for two regions from saturated velocity model, given by

**Linear region, $V_D < V_{Dsat}$**

$$I_D = \frac{q \mu_c N_D W h}{L} \left\{ 1 - \left[ \frac{(V_{bi} - V_G)}{V_{Po}} \right]^{\gamma/2} \right\} V_D$$ \hspace{1cm} (4.5)

**Saturation region, $V_D > V_{Dsat}$**

$$I_{Dsat} = \frac{q \mu_c N_D W h}{3L} V_{Po} \left\{ 1 - \frac{3(V_{bi} - V_G)}{V_{Po}} + 2 \left[ \frac{V_{bi} - V_G}{V_{Po}} \right]^{3/2} \right\}$$ \hspace{1cm} (4.6)

### 4.1.2 I-V characteristics measurement of GaAs MESFET

The I-V characteristics of 2- $\mu$m channel (device 10) and 5- $\mu$m channel (device 12) GaAs MESFET are shown in Fig. 4.2 and Fig. 4.3. The drain current is plotted against the drain voltage for various gate voltages.
Figure 4.2  \(I_{DS}-V_{DS}\) characteristics for 2-\(\mu m\) MESFET (Device #10)

Figure 4.3  \(I_{DS}-V_{DS}\) characteristics for 5-\(\mu m\) MESFET (Device #12)
4.1.3 Threshold voltage measurement

Measurement of threshold voltage from I-V characteristics

As shown in the \( I_{DS} - V_{DS} \) characteristics for different gate voltage, we see that the drain current becomes almost zero at about \( V_{GS} = -0.7 \) V for both device 10 and device 12. Reading were taken only up to this point, as if we had gone further into negative \( V_{GS} \), we would have reached a point of zero drain current at a negligible value. Therefore by these figures we get a rough estimate of the threshold voltage, which will be greater than -0.7 V, but not too greater.

Measurement of threshold voltage from linear region \( I_D - V_G \) curve

From (4.5), for linear region, \( V_D < V_{Dsat} \), we have

\[
I_D \approx \frac{\mu}{Lh} (V_G - V_T) V_D
\]

So we can plot \( I_D \) vs. \( V_G \) in the linear region, the x-intercept will be the threshold voltage \( V_T \), the plot for device #12 is shown in figure 4.4, and the threshold voltage is shown in table 4.1.

![figure 4.4](image-url)
Table 4.1  Threshold voltage calculated from $I_{DS}$-$V_{GS}$ plot in the linear region

<table>
<thead>
<tr>
<th>Device No</th>
<th>$V_D$ (V)</th>
<th>$V_T$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.4</td>
<td>-0.7</td>
</tr>
<tr>
<td>12</td>
<td>0.3</td>
<td>-0.7</td>
</tr>
</tbody>
</table>

Measurement of threshold voltage from saturation region  $\sqrt{I_D}$ - $V_G$ curve

Similarly, from (4.6), for saturation region, $V_D > V_{Dsat}$, we have

$$I_{Dsat} \approx \frac{e\mu_n W}{Lh} (V_G - V_T)^2$$  \hspace{1cm} (4.8)

We can plot $\sqrt{I_D}$ vs. $V_G$ in the saturation region and get the threshold voltage $V_T$ from the x-intercept. The plot for device #12 is shown in figure 4.5 and the calculated threshold voltage is shown in table 4.2.

![Fig 4.5 $\sqrt{I_{DS}}$ - $V_{GS}$ plot for Device #12, $V_{DS} = 3.9, 5.9$ V, ($V_{DS} > V_{Dsat}$)
<table>
<thead>
<tr>
<th>Device No</th>
<th>V_D (V)</th>
<th>V_T (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>3, 5</td>
<td>-0.9</td>
</tr>
<tr>
<td>12</td>
<td>3.9, 5.9</td>
<td>-0.9</td>
</tr>
</tbody>
</table>

Table 4.2 Threshold voltage calculated from $\sqrt{I_{DS}} - V_{GS}$ plot of saturation region

**Comparison of V_T with theoretical value calculated from implant profile**

From (4.2), the threshold voltage can be calculated from pinchoff voltage $V_{Po}$ and gate-channel built-in potential $V_{bi}$. The gate-channel built-in potential can be calculated from (4.3)

$$V_{bi} = 4.4V - \left[ 4.04V + \frac{1.42}{2} V - (0.0259V) \ln \left( \frac{7.2E16}{8.7E5} \right) \right] = 0.3V$$

Because the implantation profile is nonuniform, we cannot use (4.1) to calculate pinchoff voltage. We can read the pinchoff voltage from figure 4.6 given implantation energy and peak channel doping $N_p$.

From previous calculation in chapter 2, we get the pinchoff voltage for the channel implant $V_{Po} \approx 2.5 V$

So the threshold voltage is,

$$V_T = V_{bi} - V_{po} = 0.3 - 2.5 = -2.2 V$$

There is much discrepancy between the theoretical value and measurement results. However, from previous C-V measurement, we have

$$V_{bi} = 1.37 V$$

So the threshold voltage

$$V_T = V_{bi} - V_{po} = 1.37 - 2.5 = -1.1 V$$

Which is pretty close, so the discrepancy is caused by the poor channel implant, there may be silicon nitride layer remained or poor implantation which deteriorate the device and increase the potential barrier height and hence built-in potential.

**4.1.4 Breakdown voltage measurements**

It can be seen in the $I_{DS}$-$V_{DS}$ plot (Figure 4.6) that the breakdown voltage for $2 \mu m$ device #10 is about 17 V and for $5 \mu m$ device #12 is about 20 V.
4.2 The measurement of the electron Mobility

For low drain bias ($V_D < V_{Dss} = V_G - V_T$), the MESFET’s I-V characteristics are linear since the channel is not pinched off. From the slope of the linear region, the electron mobility can be calculated using the following equation. From (4.7)

$$
\mu_n = \frac{Lh}{\epsilon W} \frac{1}{(V_G - V_T)} \left( \frac{\partial I_D}{\partial V_D} \right)_{V_G}
$$

where

- $h$: the channel depth
- $L$ and $W$: the gate length and width
- $\left( \frac{\partial I_D}{\partial V_D} \right)_{V_G}$: the slope of the I-V characteristic curve

The measurement for three devices was shown in table 4.3-4.5

For the FatFET we measured (Large W and L MESFET)

- $L = 0.0032\text{inch} = 81.28\mu\text{m}$
- $W = 0.0080\text{inch} = 203.20\mu\text{m}$
- $h = x_j = 0.221\mu\text{m}$ (From theoretical calculation in chapter 2)
- $\varepsilon_r = 12.9$ for GaAs

$$
\varepsilon = \varepsilon_0 \varepsilon_r = 12.9 \times 8.85 \times 10^{-14} \text{Farad / m}
$$

<table>
<thead>
<tr>
<th>$V_G$ (V)</th>
<th>$\frac{\partial I_D}{\partial V_D}$ (S)</th>
<th>$\mu (cm^2/V \cdot sec)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3.70E-05</td>
<td>409.2823</td>
</tr>
<tr>
<td>-0.1</td>
<td>2.80E-05</td>
<td>361.34834</td>
</tr>
<tr>
<td>$V_G$ ($V$)</td>
<td>$\frac{\partial I_D}{\partial V_D}$ ($S$)</td>
<td>$\mu$ ($cm^2/V \cdot sec$)</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>0</td>
<td>0.0007625</td>
<td>405.11691</td>
</tr>
<tr>
<td>-0.1</td>
<td>0.0006625</td>
<td>410.65129</td>
</tr>
<tr>
<td>-0.2</td>
<td>0.0005875</td>
<td>436.99496</td>
</tr>
<tr>
<td>-0.3</td>
<td>0.003875</td>
<td>360.2884</td>
</tr>
</tbody>
</table>

**Table 4.4  Mobility for the 2 $\mu$m channel MESFET (device #10)**

For 5 $\mu$m channel MESFET (device #10)

$L = 5 \mu m$

$h = 0.221 \mu m$

$W = 104.1 \mu m$

<table>
<thead>
<tr>
<th>$V_G$ ($V$)</th>
<th>$\frac{\partial I_D}{\partial V_D}$ ($S$)</th>
<th>$\mu$ ($cm^2/V \cdot sec$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.001333333</td>
<td>1771.0029</td>
</tr>
<tr>
<td>-0.1</td>
<td>0.001066667</td>
<td>1652.936</td>
</tr>
<tr>
<td>-0.2</td>
<td>0.000886667</td>
<td>1648.8037</td>
</tr>
<tr>
<td>-0.3</td>
<td>0.000686667</td>
<td>1596.1163</td>
</tr>
</tbody>
</table>

**Table 4.5  Mobility for the 5 $\mu$m channel MESFET (device #12)**
From the theoretical calculation for the channel, we know the peak concentration $N_p$ is

$$N_p = 1.62 \times 10^{17} / cm^3$$

We can estimate the mobility using the below plot at this doping level,

![Figure 4.7 Electron mobility vs. carrier concentration](image)

The mobility is about 4400 cm$^2$/V-s. Here the discrepancy is very big. Maybe this is caused by poor channel implant.

### 4.3 Transconductance measurements

The transconductance can be calculated from the above MESFET transistor I-V characteristics, given by

$$g_m = \frac{\partial I_D(V_{GS}, V_{DS})}{\partial V_{GS}} \quad (4.10)$$

The transconductance for 2µm and 5µm MESFET at specified $V_{DS}$ is shown in table 4.6.

<table>
<thead>
<tr>
<th>Device No</th>
<th>$V_g$ (V)</th>
<th>$I_d$ (µA)</th>
<th>$g_m$ (µS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#10 ($V_{DS}=3$ V)</td>
<td>-0.2</td>
<td>0.426</td>
<td>1.04</td>
</tr>
<tr>
<td></td>
<td>-0.3</td>
<td>0.322</td>
<td></td>
</tr>
<tr>
<td>#12 ($V_{DS}=1.9$ V)</td>
<td>-0.2</td>
<td>0.415</td>
<td>1.35</td>
</tr>
<tr>
<td></td>
<td>-0.3</td>
<td>0.28</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.6 Transconductance values
4.4 Output conductance measurements

At idealized MESFET device, $I_{DS}$ is independent of $V_{DS}$ in saturation region. But in actual devices, because of channel length modulation and leakage current between source and drain, $I_{DS}$ increases as $V_{DS}$ increase. This is characterized by output conductance $g_0$, given by

$$g_o = \frac{\partial I_{DS}}{\partial V_{DS}} \bigg|_{V_{GS}} = \frac{1}{R_{DS}}$$  \hspace{1cm} (4.11)

The output conductance $g_0$ of our device is for $0.9 \times 10^{-6}$ $S$ for 2 $\mu$m device and almost constant for all $V_{GS}$, corresponding output resistance ($R_{DS}$) is of the order of $10^6$ ohm. For 5$\mu$m, $g_0$ and $R_{DS}$ are $10^{-6}$ $S$ and $10^6$ ohm respectively.

The output capacitance is important since it also affects the transit time. The output capacitance is a parasitic capacitance on the device’s output, which degrades its high frequency performance. We can calculate the output (drain-source) capacitance from the average output conductance by

$$C_{DS} = g_0 \frac{L_{eff}}{v_s}$$  \hspace{1cm} (4.12)

where

- $L_{eff}$: the effective channel length (approximate as the gate metal length)
- $v_s$: the electron velocity in the channel (approximated as $1.2 \times 10^7$ cm/sec)

For 2 $\mu$m MESFET, $C_{DS} = 1.5 \times 10^{-5}$ $pF$ and for 5 $\mu$m MESFET,

$$C_{DS} = 4.2 \times 10^{-5} \ pF$$

**Gate –Source Leakage**

With the drain open (floating), we can measure the I-V characteristic for the gate to source. We also can obtain the corresponding resistance by

$$R_i = \left( \frac{\partial I_{GS}}{\partial V_{GS}} \right)^{-1}$$  \hspace{1cm} (4.13)

The calculation results are $R_i = 4.4 \times 10^7 \Omega$ and $1.3 \times 10^8 \Omega$ for 2 $\mu$m MESFET and 5 $\mu$m MESFET respectively.

4.5 Gate - Source capacitance

We can also estimate the gate-source capacitance ($C_{GS}$) by $GSC$

$$C_{GS} \ (pF) = C_{Sc}WL$$  \hspace{1cm} (4.14)
where

\[
W = \text{gate (channel) width} \\
L = \text{gate (channel) length} \\
C_{sc} = \text{channel capacitance per area (measured in chapter 3)}
\]

For 2 μm MESFET, \(C_{GS}=0.5654\) pF and for 5 μm MESFET \(C_{GS}=1.363\) pF.

### 4.6 Source – Drain series Resistance

We can get the series resistance by

\[
R_S = \frac{\rho_{du} W}{d \cdot L} \quad (4.15)
\]

where

- \(\rho_{du}\): the resistivity of Au
- \(W\): the width of gate
- \(L\): the length of gate
- \(d\): the thickness of metal on gate

For 2 μm MESFET, \(R_S=2.28\) ohm and for 5 μm MESFET \(R_S=0.912\) ohm.

This series resistance contributes the reduction of transconductance. The extrinsic transconductance is reduced by this extrinsic series resistance. The relationship between and is given by

\[
g_m = \frac{g_{mi}}{1 + g_m R_S} \quad (4.16)
\]

where the calculated intrinsic transconductance is 5.057 (mS) for 2μm MESFET and 4.0146 (mS) for 5μm MESFET.

The gate and drain capacitance can be calculated by

\[
C_{DG} = \frac{e_o W \cdot t_m}{d_{GD}} \quad (4.17)
\]

where

- \(d_{GD}\) = separation of the gate and drain metal on GaAs surface
- \(W\) = gate width perpendicular to current flow
- \(t_m\) = thickness of pad metal

The result value is 0.0381 pF.

### 4.7 MESFET Small Signal Equivalent Circuit

The small signal equivalent circuit for the MESFET can be assembled from the above measurements and calculations as shown in figure 4.8. The data is shown table 4.7.
and 4.8.

Figure 4.8 Small equivalent circuit for MESFET

From the above measurement and calculations, we can assemble the small signal equivalent circuit for MESFET. We choose the DC point at $V_{DS}=3 \text{ V}$ for device #10 $V_{DS}=1.9 \text{ V}$ for device #12, $V_{GS}=-0.3\text{V}$.

For 2 $\mu$m MESFET,

<table>
<thead>
<tr>
<th>Intrinsic Element</th>
<th>Extrinsic Elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_m=1.04 \text{ } (\mu\text{S})$</td>
<td>$C_{DS}=1.5 \times 10^{-5} \text{ pF}$</td>
</tr>
<tr>
<td>$CGS=0.5654(\text{pF})$</td>
<td>$R_g=2.28(\Omega)$</td>
</tr>
<tr>
<td>$R_d=10000(\Omega)$</td>
<td>$R_d=1.43(\Omega)$</td>
</tr>
<tr>
<td>$R_i = 4.4 \times 10^7 \Omega$</td>
<td>$R_s=1.43(\Omega)$</td>
</tr>
<tr>
<td>$C_{DG}=0.0381 \text{ (pF)}$</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.7 Small equivalent circuit elements for 2 $\mu$m MESFET

For 5 $\mu$m MESFET,
<table>
<thead>
<tr>
<th>Intrinsic Element</th>
<th>Extrinsic Elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_m = 1.35 \mu S$</td>
<td>$C_{DS} = 4.2 \times 10^{-5} \ pF$</td>
</tr>
<tr>
<td>$C_{GS} = 1.363 \ pF$</td>
<td>$R_g = 0.912 \ \Omega$</td>
</tr>
<tr>
<td>$R_d = 20000 \ \Omega$</td>
<td>$R_d = 1.43 \ \Omega$</td>
</tr>
<tr>
<td>$R_i = 1.3 \times 10^6 \ \Omega$</td>
<td>$R_s = 1.43 \ \Omega$</td>
</tr>
<tr>
<td>$C_{DG} = 0.0381 \ pF$</td>
<td></td>
</tr>
</tbody>
</table>

The small equivalent circuit for 2 µm is shown in Fig. 3.32

4.8 Cutoff Frequency

The cutoff frequency $f_T$ is maximum frequency at which the transistor can operate with gain and is given by

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})}$$

The cutoff frequencies obtained in our devices are $f_T = 1.32\text{MHz}$ for 2 µm MESFET and 3.96MHz for 5 µm MESFET. In general, the maximum cutoff frequency is related to the transit time effect. Therefore, in order to obtain a more desirable and higher cutoff frequency, the output resistance and the parasitic source to drain resistance must be minimized to achieve a higher transconductance. The output capacitance should also been reduced. Furthermore, improvement of the fabrication and measuring techniques in our lab should be made.
Chapter 5 Conclusion

In this Fabrication Lab course, we fabricated the GaAs MESFETs using a simple four-mask, double ion implantation process. This process includes the standard process of photolithography, ion implantation, and metal deposition.

After fabrication, we did the sheet resistance measurements, channel and source/drain I-V measurements, TLM measurements, I–V characteristic of Schottky diode measurements, breakdown measurements, C-V measurements, MESFET I-V measurements, threshold voltage measurements, trans-conductance measurements, Electron mobility measurements, Output conductance measurements, gate source leakage measurements, and optical measurements for some devices.

After dealing with the experimental data, we found most of the obtained data from experiments are consistent to the theoretical results. This testifies the theories to describe the fabrication process and the characteristics of these devices are correct. Also the results verified that we did the correct fabrication process and obtained the devices with good quality and did the correct measurements.

From this class, we learn the comprehensive knowledge in fabrication and in the various characteristics for MESFET devices. This gave us a much deeper comprehension in this field and will surely help us in the future learning and working.

We would like to appreciate Prof. Kenneth P. Roenker for his perfect lectures. And we also want to give our thanks to the engineer and the TA for this class for their good help.